BUDAPESTI MŰSZAKI ÉS GAZDASÁGTUDOMÁNYI EGYETEM

Villamosmérnöki és Informatikai kar

Extending the thermal transient testing methodology for reliability testing of power electronics components

PhD Thesis-Booklet

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Motivation

One of the main challenges of our time is to mitigate the effects of climate change and build a more sustainable future. This aspiration gave a great momentum to the renewable energy generation and electrification of transportation and generated a great demand for the development of medium and high-power AC-DC, DC-DC and DC-AC power converters. To increase the efficiency and power density of these modules, all components must be thoroughly optimized for the application. In my work, I was mostly focusing on the main switching power transistors and power transistor modules, which are critical components of the converters. Most used devices are MOSFET transistors at moderate power levels, while at high voltage and power applications the IGBTs, but at the highest power levels various thyristor types are still widely used. Besides the main electronics operation the long-term reliability of these components is just as important in the above-mentioned applications. Investigations shown that the failure of electronics systems are caused by thermal related issues in majority of the cases.

Identified Problems Requiring Novel Solutions

Throughout the operation of the power converters, power semiconductor components are subjected to periodic temperature changes. Power cycling is one of the most important test methods for thermal reliability testing of power electronics components, which achieves repeated heating and cooling cycles in the component by applied periodic electric excitations. This load mimics the active operation cycles of the components and through due to the periodically arising thermomechanical stresses lead to the degradation of primarily the interface layers. These tests are often used to serve input data for lifetime curve fitting by running the test until the device fails and noting the number of cycles elapsed until failure. Often only very basic process monitoring is used, capturing minimum and maximum temperatures and voltages, which are required only to detect the end-of-life criteria. However, with more sophisticated measurement approaches the degradation process of the various interface layers could be monitored as well and the acquired data used to improve the module design and/or manufacturing technology. Most of such diagnostic measurement approaches requires interrupting the power cycling and moving the sample to the laboratory for testing. This makes these tests time consuming and expensive. There is a demand for integrating the power cycling and the diagnostic test systems. Thermal transient testing technique relies on measuring the step response of a temperature dependent electrical parameter of the semiconductor chip to characterize its heat flow path and extract a model proportional to the physical structure of the package and cooling environment. As this test method requires only electrical connections to the tested device, its integration with the power cycling system opens new opportunities.

The silicon-based power device technology is approaching to reach the limits of the silicon material, and hence the research and development of wide bandgap material-based transistor devices have accelerated, especially in case of Silicon Carbide (SiC) and Gallium Nitride (GaN) materials. For the thermal characterization of the SiC MOSFETs and diodes the proper test methodology is already solved, but due to their unique structure measurement of GaN HEMT devices is an open challenge and simulation is still the primary tool for thermal characterization of GaN HEMT devices with limited experimental support.

In a power switching application not only the semiconductor components, but capacitors are also suffering from considerable thermal load. Both the heat generated by the surrounding components and power losses generated on the capacitor itself contribute to elevated temperature of the capacitor which can have negative effect on the electrical parameters and lifetime as well. Most of the published measurement solutions utilize temperature sensors attached to the case surface embedded thermocouples or other temperature sensors, use infrared temperature sensors focused on a dedicated point on the casing of the component or simply use IR camera to measure the case temperature. All these approaches are altering the device structure or limited to measure only surface temperature. Adapting electrical test method and thermal transient testing could provide new opportunities for testing capacitances in hard-to-reach locations e.g., embedded capacitors.

Research Objectives

During my research activity I attempted to reach three main goals:

- Improve power cycling tests with integrated thermal transient testing, to allow collecting diagnostics data frequently during the full testing process and assess how the captured can be utilized to detect and identify various failure modes.

- Extend thermal transient testing and power cycling capabilities to GaN HEMT devices by elaborating new device specific electrical setups.

- Assess if thermal transient testing methodology can be applied for the characterization of discrete capacitor components as well.

In my doctoral work I was focusing on improving the power cycling reliability test method by combining with thermal transient testing and extending the applicability of this new test method to new device types.

Methodology

In all my experiments I used the Simcenter Micred T3Ster system for capturing the thermal transient response of the measured component. In the early experiments I used a desktop hardware setup with the main T3Ster system and additional power driving extensions (so called Boosters) and a self-made control software to carry out both the power cycling and the thermal transient tests as well. Later, based on the good initial results and great market interest Mentor Graphics released their power cycling system with integrated thermal transient testing capability, called Simcenter Micred Power Tester. Majority of the power cycling measurement results presented below were generated using this commercial equipment.

To adapt the thermal testing capability to new device types, GaN HEMTs and capacitor components, I had to extend the Main T3Ster unit with custom auxiliary circuitry, ranging from just a few passive components to smaller preamplifier circuits or reference voltage sources. In the dissertation I provided the high-level schematics of the measurement setups in each case.

1 Research topic: Separation of the main failure modes in power cycling tests combined with thermal transient testing

In the first section of my thesis, I propose a new test setup by integrating power cycling with thermal transient testing as structural investigation method. The combination of the two technologies allows us to monitor the degradation of the internal structure of the component without significantly increasing total test time. This information can help us better understand the formation of the various failure modes, and hence provide useful feedback for the optimization of manufacturing and improving the design. I demonstrate how the captured data can be used to identify various failure modes and propose a method to separate the effect of concurrently arising failure mechanisms.

Thesis 1.

I proposed a new power cycling solution by integrating thermal transient measurement as a nondestructive structural investigation method with power cycling. The integration of the two methods allows frequent, detailed monitoring of the structure, hence collecting much more information on the development of various failure modes without significantly affecting the total test time.

Thesis 1.1

I confirmed through a series of targeted experiments that various failure modes in the heat flow path can be detected using the frequently captured structure functions. The propagation of both die-attach degradation and the deterioration of further attachment layers can be identified and distinguished.

Thesis 1.2

I proved experimentally that the stepwise changes experienced on the long term on-state voltage graphs captured during the power cycling tests correspond to the break/detachment of individual bond wires.

Thesis 1.3

I proposed a compensation method for the on-state voltage graph to separate the effects of concurrently forming structural degradation in heat flow path and the deterioration of bond wire resistances. The compensation factor considers the change of the peak junction temperature and the temperature dependence of the device voltage at heating current.

2 Research topic: Thermal transient testing of GaN based semiconductor devices

In the second section of my dissertation I attempt to extend the method described in the first section to GaN HEMT devices. In order adapt the combined test method for a new device type, first we must ensure that we can capture high fidelity thermal transient response of the component. I demonstrate that classic measurement methods used for silicon devices, most of the times, cannot be applied for testing HEMT devices. Moreover, due to the wide range of device variants, there is no single measurement method that can be used for all variations. I propose four different measurement setups for the testing of various device types including HEMT devices optimized for RF power amplifier applications, cascode HEMT devices and HEMTs with enhancement mode characteristics. These measurement setups are applicable not only for thermal characterization, but for power cycling as well.

Thesis 2.

I elaborated new methods and measurement setups for the thermal transient testing of various depletion mode and enhancement mode GaN HEMT types to allow thermal characterization and power cycling of these components.

Thesis 2.1

I proposed a new thermal transient test setup for the thermal testing of classic, depletion mode GaN HEMT devices. The setup utilizes the forward voltage of the gate Schottky contact as temperature sensitive parameter, while the heating current is applied on the on-state channel resistance.

Thesis 2.2

For the characterization of GaN HEMT power amplifiers I proposed an extension for 2.1 measurement setup. The added feedback loop allows reducing gate voltage during the heating to increase the heating power at limited current while maintaining stable operating point.

Thesis 2.3

I elaborated a new thermal transient measurement method for the thermal testing of cascode type enhancement mode power HEMT devices. The method utilizes multiple thermal transients measured on the body diode of the MOSFET and the on-state channel resistance of the two chips and an iterative compensation algorithm.

Thesis 2.4

I adapted 2.1 measurement setup for enhancement mode GaN devices with reduced gate leakage current, by using the gate current as temperature dependent electrical parameter. I confirmed the validity of the new measurement method by simulation results.

3 Research topic: Thermal transient testing of discrete capacitors

In my third research topic I examine the possibility of extending thermal transient testing methodology for capacitor components as well. In a power switching application not only the semiconductor components, but capacitors are also suffering from considerable thermal load. I propose a measurement setup which enables us to use the capacitance of smaller discrete capacitors as temperature dependent electric parameter. I demonstrate the operation of the test circuit in measuring thermal transient responses caused by transfer heating of neighboring component and heat generated on the capacitor as well. Finally, I use detailed 3D CFD thermal simulation to validate the measurement results. Already with the initial model parameters a good match between the simulated and measured data could be seen, but comparison of the transient responses allowed fine tuning uncertain model parameters as well.

Thesis 3.

I proposed a new method for the thermal characterization of discrete capacitor components by adapting the thermal transient measurement method. By using a switched capacitor circuit, I turned the tested capacitor into an equivalent resistance, whose value depends on the capacitance and hence the temperature of the capacitor. By applying constant current load on this circuit, the transient change of the resulting voltage drop can be measured as a temperature dependent electric parameter.

Thesis 3.1

I developed a method for the calibration of the measured voltage signal. I put the measured capacitor into temperature-controlled environment and applied the load current at t=0s. I used and exponential curve fitted to the early section of the measured transient to extrapolate to the voltage corresponding to the t=0s time.

Thesis 3.2

I proved experimentally that the above-described measurement and calibration methods can be used to measure both the thermal self-impedance of a capacitor, and the temperature change caused by the heating effect of surrounding components as well.

Thesis 3.3

I confirmed the validity of the captured thermal transients by 3D CFD simulations. The measured and simulated transients showed good match. Based on the differences of the two transient curves the uncertain parameters causing the differences can be identified and fine-tuned. This way the measured transients can be used to improve the accuracy of the simulation model as well.

Industrial application of the research results

Most of my research activities were carried out in connection with my work at Mentor Graphics (Siemens) and were initiated and motivated by industry needs. Some of them even inspired actual product development.

The results of my first research topic were used as the basis of the development of Simcenter Micred Power Tester, an industrial implementation of the integrated power cycling and thermal transient testing concept, and provide guideline for the customers on how to interpret and utilize the data acquired with the system. Many industry leading power electronics companies have adapted and are using the presented solutions today in their processes to develop and validate the reliability of new discrete package and power module solutions.

The measurement methods elaborated in the second research topic enabled number of customers to greatly improve their GaN HEMT testing capabilities and validate or improve their simulation models as well. With the spreading of the GaN technology more and more companies are expected to benefit from these measurement solutions.

Publications corresponding to research topics

1 Research topic:

1. **Z. Sarkany, M. Rencz, “Methods for the Separation of Failure Modes in Power-Cycling Tests of High-Power Transistor Modules Using Accurate Voltage Monitoring”, Energies 2020, 13(11), 2718; doi: 10.3390/en13112718**
2. M. Rencz, G. Farkas, **Z. Sarkany**, A. Vass-Varnai,.”The Use of Thermal Transient Testing” In: Rencz, M., Farkas, G., Poppe, A. (eds) Theory and Practice of Thermal Transient Testing of Electronic Components. Springer, Cham. (2022) https://doi.org/10.1007/978-3-030-86174-2_7
3. **Z. Sarkany** and M. Rencz, "The influence of the cycling parameters on the reliability test results of IGBTs," 2017 IEEE 19th Electronics Packaging Technology Conference (EPTC), Singapore, 2017, pp. 1-4, doi: 10.1109/EPTC.2017.8277513.
4. C. A. Manier, H. Oppermann, L. Dietrich, C. Ehrhardt, **Z. Sarkany**, M. Rencz, B. Wunderle, W. Maurer, R. Mitova, K. D. Lang, "Packaging and Characterization of Silicon and SiC-based Power Inverter Module with Double Sided Cooling," PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2016, pp. 1-8.
5. **Z. Sarkany**, Weikun He and M. Rencz, "Temperature change induced degradation of SiC MOSFET devices," 2016 15th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems

(ITherm), Las Vegas, NV, USA, 2016, pp. 1572-1579, doi: 10.1109/ITHERM.2016.7517736.

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8. **Z. Sárkány**, A. Vass-Várnai and M. Rencz, "Separation of failure modes in short cycle time power cycling experiments," 20th International Workshop on Thermal Investigations of ICs and Systems, Greenwich, UK, 2014, pp. 1-5, doi: 10.1109/THERMINIC.2014.6972528.
9. **Z. Sarkany**, A. Vass-Varnai and M. Rencz, "Analysis of concurrent failure mechanisms in IGBT structures during active power cycling tests," 2014 IEEE 16th Electronics Packaging Technology Conference (EPTC), Singapore, 2014, pp. 650-654, doi: 10.1109/EPTC.2014.7028349.
10. **Z. Sarkany**, A. Vass-Varnai and M. Rencz, "Investigation of die-attach degradation using power cycling tests," 2013 IEEE 15th Electronics Packaging Technology Conference (EPTC 2013), Singapore, 2013, pp. 780-784, doi: 10.1109/EPTC.2013.6745827.
11. **Z. Sarkany**, A. Vass-Varnai, G. Hantos and M. Rencz, "Failure prediction of IGBT modules based on power

cycling tests," 19th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), Berlin, Germany, 2013, pp. 270-273, doi: 10.1109/THERMINIC.2013.6675197.

2 Research topic:

1. G. Farkas, A. Poppe, **Z. Sarkany**, A. Vass-Varnai, “Thermal Transient Measurements on Various Electronic Components” In: Rencz, M., Farkas, G., Poppe, A. (eds) Theory and Practice of Thermal Transient Testing of Electronic Components. Springer, Cham. (2022). https://doi.org/10.1007/978-3-030-86174-2_6

2. **Z. Sarkany** et al., "Thermal transient testing alternatives for the characterization of GaN HEMT power devices," 2022 28th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), Dublin, Ireland, 2022, pp. 1-4, doi:10.1109/THERMINIC57263.2022.9950647

3. G. Farkas, **Z. Sarkany** and M. Rencz, "Issues in Testing Advanced Power Semiconductor Devices," PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2016, pp. 1-8.

4. **Z. Sarkany**, G. Farkas and M. Rencz, "Thermal transient characterization of pHEMT devices," 18th International Workshop on THERMal INvestigation of ICs and Systems, Budapest, Hungary, 2012, pp. 1-4.

3 Research topic:

1. **Z. Sarkany, M. Rencz, "A Way for Measuring the Temperature Transients of Capacitors", Advances in Science, Technology and Engineering Systems Journal, vol. 2, no. 3, pp. 1381-1389 (2017), doi: 10.25046/aj0203174**
2. **Z. Sarkany** and M. Rencz, "A way for measuring the temperature transients of capacitors," 2016 IEEE 18th Electronics Packaging Technology Conference (EPTC), Singapore, 2016, pp. 818-822, doi: 10.1109/EPTC.2016.7861594.
3. [1]**Z. Sarkany**, G. Farkas and M. Rencz, "Thermal characterization of capacitors," 2016 International Conference on Electronics Packaging (ICEP), Hokkaido, Japan, 2016, pp. 200-203, doi: 10.1109/ICEP.2016.7486811.
4. **Z. Sarkany**, G. Farkas and M. Rencz, "Thermal resistance measurement of discrete capacitors," 2015 IEEE 17th Electronics Packaging and Technology Conference (EPTC), Singapore, 2015, pp. 1-5, doi: 10.1109/EPTC.2015.7412332.

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[1] The organizing committee of the conference selected this paper to win the Best Paper Award

Publications not directly related to thesis

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2. **G. Farkas, Z. Sarkany, M. Rencz, "Structural Analysis of Power Devices and Assemblies by Thermal Transient Measurements", Energies. 2019; 12(14):2696. dio: 10.3390/en12142696.**
3. **A. Vass-Varnai, Z. Sarkany, M. Rencz," Characterization method for thermal interface materials imitating an in-situ environment", Microelectronics Journal (0026-2692 0959-8324): 43 9 pp 661-668 (2012), doi: 10.1016/j.mejo.2011.06.013.**
4. S. Ress, **Z. Sarkany**, G. Farkas and M. Rencz, "Accelerating the Thermal Transient Testing by a Novel Temperature Sensitive Parameter Calibration Method based on I-V Characteristic Measurement," 2022 28th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), Dublin, Ireland, 2022, pp. 1-4, doi: 10.1109/THERMINIC57263.2022.9950658.
5. S. Ress, **Z. Sarkany**, G. Farkas and M. Rencz, "On the Correction of the Effects of Electrical Transients in the Measured Thermal Transients," 2021 IEEE 23rd Electronics Packaging Technology Conference (EPTC), Singapore, Singapore, 2021, pp. 399-404, doi: 10.1109/EPTC53413.2021.9663887.
6. A. Poppe, A. Vass-Varnai, **Z. Sarkany**, M. Rencz, G. Hantos and G. Farkas, "Suggestions for Extending the Scope of

the Transient Dual Interface Method," 2021 27th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), Berlin, Germany, 2021, pp. 1-8, doi: 10.1109/THERMINIC52472.2021.9626508.

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8. G. Hantos, J. Hegedus, M. C. Bein. L. Gaal, G. Farkas, **Z. Sarkany**, S. Ress, A. Poppe, M. Rencz, "Measurement issues in LED characterization for Delphi4LED style combined electrical-optical-thermal LED modeling," 2017 IEEE 19th Electronics Packaging Technology Conference (EPTC), Singapore, 2017, pp. 1-7, doi: 10.1109/EPTC.2017.8277493.
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10. A. Szel, **Z. Sarkany**, M. Bein, R. Bornoff, A. Vass-Varnai and M. Rencz, "Mission profile driven component design for adjusting product lifetime on system level," 2015 International Conference on Electronics Packaging and iMAPS All Asia Conference (ICEP-IAAC), Kyoto, Japan,

2015, pp. 385-389, doi: 10.1109/ICEP-IAAC.2015.7111041.

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15. **Z. Sarkany** and M. Rencz, "Investigation of nonlinear thermal parameters of compound semiconductor devices," 2013 Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP), Barcelona, Spain, 2013, pp. 1-5.

16. A. Vass-Varnai, S. Laky, **Z. Sarkany**, C. Barna and M. Rencz, "Issues of finding a proper golden-reference sample for TIM tester calibration," 29th IEEE Semiconductor Thermal Measurement and Management Symposium, San Jose, CA, USA, 2013, pp. 200-205, doi: 10.1109/SEMI-THERM.2013.6526829.
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18. A Vass-Varnai, B Plesz, **Z Sarkany**, A Malek, M Rencz, “Application of Thermal Transient Testing for Solar Cell Characterization” In: Proceedings of the 28th IEEE Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM'12).San Jose, USA, 2012.03.18-2012.03.22., pp. 162-168. 978-1-4673-1109
19. A. Vass-Varnai, **Z. Sarkany**, G. Farkas, Marta Rencz, “Industrial Need for Accurate and Reproducible Measurements of Thermal Interface Materials”, In: International conference on Electronics Packaging, ICEP-IAAC 2012. Tokyo, Japan, 2012.04.17-2012.04.20. Tokyo: pp. 524-531.
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