



M Ű E G Y E T E M 1 7 8 2

Budapest University of Technology and Economics

Department of Electronics Technology

MODELING THE SOLDERING PROCESS OF SURFACE MOUNT PASSIVE COMPONENTS AND MECHANICAL INVESTIGATION OF THE JOINTS

PHD THESIS

Krammer Olivér

Head of department: Dr. Harsányi Gábor

Tutor: Dr. Illyefalvi-Vitéz Zsolt

BUDAPEST

2010

Preliminaries

Reflow soldering is generally used for mechanical fastening and electrical joining of components to electronic circuit assemblies. In mass production, at first solder paste, which is a suspension containing powder of solder alloy and flux, is printed onto the surface of the assembling board through a metal mask, called stencil. The apertures of the metal mask are made in exact position, shape and volume, according to the soldering pads of the board. Then components are placed onto the board, pushing their terminals into the printed paste. The third step is the preparation of the joints by heating and melting – reflowing – the solder paste in conveyor type forced convection reflow ovens.

The passive discrete components (resistors and capacitors) are getting smaller and smaller as it is demanded by the continuous development of surface mount technology. Similarly, the distance between the leads of integrated circuit packages is also decreasing; consequently automated assembling machines are facing real challenges. The evaluation of the accuracy of the component placement systems has become important because the reduction of components sizes leads to a lower relative accuracy of their positions by the application of the same placing speed. Therefore the question has arisen what is the effect of the positioning inaccuracy on the reliability of the solder joints? It is an empirical fact that the inaccuracy of placement can be reduced to a certain extent by the self-alignment of the components, because the surface tension of the molten solder pulls the components towards the right position. The precondition of the self-alignment is that the volume and shape of the solder paste deposited by stencil printing onto the soldering pads should be optimum.

To improve the quality and reliability of circuit board assemblies, the analysis of the processes and effects described above has a great importance. After reviewing the relevant literature I have found to many neglects, even lacks in the research results of these fields. That is why I chose the topic for my thesis work to investigate the soldering process and examine the quality of solder joints of small discrete surface mounted components.

Open issues of the research area

The mechanical strength of solder alloys is mainly characterized by their tensile and shear strength. In case of bulk samples the tensile strength [1] is used for the characterization, while in case of more complex structures (real soldered joints) only the shear strength can be measured [2,3]. If the determination of the contact surface between the solder joint and the component metallization is difficult or impossible, like in case of small passive components, the shear strength is characterized by the maximum force needed for the fracture of the joint instead of the maximum of the stress [4,5].

However this characterization calls forth various problems. On one hand the results are not comparable in case of different sizes of the components and different shapes of the joints. On the other hand, if the components have position offset after soldering, the joint shape depends not only on the topology of the contact surfaces but on the extent of the position offset as well. The effect of the position offset on the mechanical strength of the joints has not been analyzed yet.

At the beginning phase of surface mount technology, the examination of the self-aligning movement of the components during reflow soldering was limited to passive discrete components of larger sizes e.g. components with size code 1206¹ (3 x 1.5 mm). At that time the applied models were two-dimensional and mainly focused on the tomb-stone effect (when one of the terminations of the component lifts from the pad). Although the movement parallel to the lengthwise axis of the components could be described by these models, the perpendicular movement could not be characterized [6,7]. Later, when the more complex surface mounted integrated circuit packages, e.g. the QFP (Quad Flat Pack) and the BGA (Ball Grid Array) packages were put into use. Consequently these components were got into the focus of investigations and still hold for the main direction of researches today [8,9]. Since the decrease in the size of surface mounted passive discrete leads to the increase of the positioning offset derived from the inaccuracy of the pick and place machines, a novel and detailed analysis of the self-aligning movement of components during the soldering is required.

The application of very small components also implicated the examination of the stencil printing process. Current researches at this field focus on the stencil topologies used for fine-pitch components [10]. Furthermore the effect of the

¹ According to the industrial practice, I use the coding based on the English units to describe the dimensions of small passive discrete components, with indicating the metric units as well.

properties of the solder paste, the squeegee and the printing process on the quality of the created deposits have also been analyzed [11,12].

The volume of the deposited solder paste affects both the self-alignment of components and the mechanical strength of the solder joints in case of small sized passive discrete components. In case of gasket failure, when there is a gap between the stencil and the board, because the stencil is not fit tightly to the board during printing, the volume of the deposited solder paste can be greater than expected, even asymmetric on the sides of the component. This can implicate component skewing during soldering if the forces coming from the surface tension of the molten solder paste are not balanced at the two terminations of the components. Furthermore the increased volume of the soldering paste can cause the appearance of solder bridges between the leads of fine-pitch components.

The gasket failure of the stencil foil can be caused by the level differences on the surface of the board, for example the higher level of copper tracks coated by solder mask or the identifier decals. If these level differences are not too big or laterally they are far enough from the soldering pads, then the stencil foil can bend down to the board during stencil printing and the volume of the deposited paste will be the same as the expected amount. The standard IPC-7525 describes (for the usage of step-stencils in a similar application field) what minimum distance should be held between a stencil aperture of a soldering pad and the stencil-step so that the difference between the stencil levels does not lead to a printing failure. However this standard provides only a rough design guideline² because the thickness of the stencil foil is not taken into consideration although it has an effect on the deformation of the stencil. The influence of the surface level differences of the board on the quality of the printed deposits and on the deformation of the stencil during printing has not been examined yet.

² The minimal distance should be the step-height multiplied by 36.

The aim and the method of my research

The following goals were set for my work in order to provide solutions for the problems and open issues of the research area:

- developing a measurement method where the shear strength of the surface mounted passive discrete components having a position offset can be characterized by the stress instead of the force,
- determining the influence of the position offset on the shear strength,
- analyzing the self-alignment movement of the surface mounted passive discrete components during reflow soldering,
- defining a measurement method which is able to describe the effect of the level differences of the board on the quality of stencil printing,
- providing design guidelines which help to prevent the effect of the level differences of the board on the volume of the solder paste deposits.

In order to investigate the solder joints of components with position offset and to measure this position offset correctly, I placed reference patterns next to the soldering pads on my experimental boards. The position offset of the components was measured by optical microscope having a resolution of 4 μm . The 3 dimensional calculation of the solder profile was performed by specific free accessible software which calculated the shapes of fluids based on the principle of the minimum energy: it minimized the energy coming from the surface tension and the gravity. The input parameters for the 3 dimensional calculation of the solder profile were gathered from measuring the cross-section of real solder joints. The calculations for the case of components with position offset were validated also by analyzing the cross-section of real solder joints after that. The shear load of solder joints was performed by industrial measurement equipment designed especially for this. The speed of the load was 100 $\mu\text{m/s}$ corresponding to industrial applications. For the mechanical simulation of solder joints the input material parameters were obtained from the literature while the shape of the solder joints were calculated by the 3 dimensional calculations. I created an own measuring equipment to measure the deformation of the stencil which also served as input parameters for the simulation. The stencil and the printing squeegee respectively were loaded by different weights using the scale-beam of my measuring equipment. The deformation of the stencil and the vertical movement of the squeegee were measured by a micrometer clock having a resolution of 10 μm . The average deviation was 50 μm in the measurement interval of 0-2 mm. The mechanical simulation of the stencil was performed via a model based on the Finite Element Method where the input material parameters were extracted from the results of the measurements.

New scientific results

Part I: Mechanical investigation of solder joints of surface mounted passive discrete components

Thesis I/1: I have developed a method which characterizes the shear strength of solder joints of small passive discrete components based on the average stress instead of the loading force.

Two input data are required to determine the average stress induced by the shearing load in the solder joint at the moment of the crack: the maximal loading force which causes the crack and the joint surface, which is the area of the solder joint where it is connected to the metallization of the component body. The main idea behind my method is the calculation of the (otherwise hardly calculable) joint surface by a 3 dimensional profile calculation based on the minimization of the inner energy of the solder alloy. The joint surface depends mostly on the volume of the solder paste, the material properties of the metals participating in the soldering, the dimensions and the position of the component. While the volume of the solder paste and the material properties are given, the position of the component depends on the accuracy of the component placement. Therefore to determine the joint surface I measured the final position of the component after soldering. Applying my method the shear strength of the surface mount discrete components with an offset can be determined and the results of the experiments using components of different shape and size can be compared.

Corresponding results were published in: L1, R3, K1, K2

Thesis I/2: By executing experiments and applying computer simulation I have proved that the shear load induces higher stress in the solder joints of chip components if their position offset is larger.

The shear strength of soldered joints of components with an offset was calculated by the method presented in I/1. For my investigations I designed an experimental board, which was suitable for being populated with 90 pieces of small surface mounted discrete resistors (size code 0603 – 1.5 x 0.75mm). The thickness of the experimental board is 1.5 mm and it is made of class FR4 glass fiber epoxy. The soldering surfaces were made of a 35 μm thick copper layer covered by a 0.1–0.2 μm thick silver layer deposited by an immersion process. The resistors were misplaced intentionally with a pick and place machine. Before placing the components, heat curable glue was dispensed to the position of the components to fasten them to the board so that they cannot be moved by the surface tension of the molten solder

during soldering. The intentional discrete position offsets were in the range 0 and 250 μm . I designed reference patterns made of the same copper layer on the experimental board next to the soldering pads. After soldering, the position offsets were measured in relation to these reference patterns. The measurement of the maximum shearing force was performed on a pre-defined higher temperature level (90 °C) so that the results were not influenced by the glue which fastened the components to the board. From the results I drew the conclusion that the shear strength of the solder joints of components having position offsets was definitely lower than in the case when the components had no position offset. At a position offset of 250 μm the shear strength was 12-17 MPa, while with no position offset it was about 26 MPa.

The results were also verified by calculations using finite element method (FEM) model. The 3 dimensional profiles, which were calculated for the measurements, were added into a FEM model. First, the displacement of the solder shape affected by the maximal shear force was calculated for a component placed in the right position. Then the stress in the solder joint caused by the position offset was calculated for offsets of different extents. Based on the simulation results the shear strength in the solder joint caused by an identical amount of load increased proportionally to the extent of the position offset; it was 68 MPa in case of having a position offset of 250 μm and it was 35 MPa in case of having no offset.

Corresponding results were published in: L1, R3, K1

Part II: Investigation the movement of surface mounted passive discrete components during reflow soldering

Thesis II/1: I have created a 3 dimensional theoretical model for showing by computer simulation that the self-aligning ability parallel with the lengthwise axis of the component is lower than it is in the lateral direction; this phenomenon was validated by experiments as well.

The experimental board presented in Thesis I/2 was applied for the measurement. Small passive discrete resistors having the size code 0603 were placed also intentionally to positions with offset. The offset of the components was measured before and after soldering using optical microscopy. Based on the measured results I showed that the self-aligning ability parallel with the lengthwise axis of the component is lower than it is in the lateral direction; for example it was 170 μm in the lengthwise direction for a component having a position offset of 300 μm while it was 240 μm in the lateral direction.

The theoretical reason of the lateral self-alignment is that this movement is caused by the forces originating from the surface tension of the molten solder at both sides of the components perpendicular to the axis. In contrary, the lengthwise self-alignment of the components is caused by the hydrostatical and capillary pressures acting on the face metallization as well as the lengthwise force components of the surface tension, and the resulting force makes the components move. The explanation for the lower self-alignment capability in this case is, that the forces acting on the metallized faces of the component are pointing to the opposite directions and consequently only their difference makes the component move into the lengthwise direction.

Corresponding results were published in: L2, R3, R4, R5

Thesis II/2: By applying the model presented in II/1. and using simulations I have shown that the lengthwise self-alignment of the components is improved when at both terminations of the component there is solderable metallization on the sidewalls in addition to the metallization on its bottom, face and top.

The experimental board presented in Thesis I/2 was applied for the measurement. The terminations of the capacitors (of a type of commercial small passive discrete components) have metallization also on the sidewalls, while resistors (the other type of similar components) have metallization only on their bottom, top and face. Therefore I placed resistors and also capacitors onto the board to validate the theoretical statements. I measured the position of both types of components before and after soldering. Because the weight of the capacitors is greater than that of the resistors, my results were weighed also by the mass of the components. Hence the measurement unit of the resulting quantity, which characterizes the self-aligning ability, is $\mu\text{m}\cdot\text{mg}$. Considering the results the following can be stated: if the position offset of the components is lengthwise then the self-aligning ability of the capacitors (with sidewall metallization) is significantly higher. For example it was 1300 $\mu\text{m}\cdot\text{mg}$ for capacitors and only 420 $\mu\text{m}\cdot\text{mg}$ for resistors with having position offsets of 370 μm in both cases.

The theoretical explanation of this phenomenon is that if there is metallization also on the sidewalls of the terminations of the components then the contact angle of the force originating from the surface tension depends on the extent of the lengthwise position offset of the component. When the position offset of the component is higher and higher, the direction of the force originating from the surface tension points more and more to the center of the component which definitely helps its self-alignment.

Corresponding results were published in: L2, R3

Part III: The effect of the level differences of the board on the quality of the stencil printed paste deposits.

Thesis III/1: I have created a method to determine the effect of the level differences of the board on the height and on the area of the stencil printed paste deposits.

The main idea behind my method is the application of a test board containing possible level differences. The test board is designed and fabricated to have specific thickened surfaces made by electroplating in the direct neighborhood of the soldering pads. I designed three boards having electroplated surfaces with different thicknesses of +25, +55, +90 μm in addition to the original thickness of the soldering pads. The height of the printed paste deposits was measured by a 3D paste inspection machine with a resolution of 1 μm , while the area of the deposits was calculated in the photos made by optical microscopy.

Based on the experiments it can be stated that the area of the deposits increases significantly if the stencil cannot bend onto the board during printing. For example the area of the paste deposit increased from 0.25 mm^2 (which was equal to the area of the stencil aperture) to 0.41 mm^2 , when the level difference was +90 μm .

Furthermore based on the experimental results it can also be stated that the height of the paste deposits equals to the sum of the thickness of the stencil foil (150 μm) and the level differences on the bare board if the electroplated area is close enough to the soldering pad (0.3–3 mm). Moreover the stencil bends down to the soldering surface and the height of the paste deposits equals to the thickness of the stencil foil if the level difference is far enough from the soldering pad (6–12 mm).

Corresponding results were published in: R1, R2

Thesis III/2.: With the aim of computer simulation I have determined the necessary minimum distance between the level differences of the board and the soldering pad for different stencil foil thicknesses (75-175 μm) to get the stencil be able to bend down completely to the soldering pads. The minimum distance in the range of 0–60 μm level difference is: $C \cdot d \cdot h$ (C – constant: 1.6 [$1/\mu\text{m}$], d – stencil foil thickness, h – level difference).

For the investigation I have created a Finite Element model, for which the input parameters of the elasticity of the stencil and of the squeegee were determined by deformation measurements. For the deformation measurements I created an own

measuring equipment, which was able to determine the deformation of the stencil and of the squeegee at different values of load. I verified the FEM model by comparing simulation results to the experimental results of Thesis III/1. Then I inserted different level differences (0–90 μm) into the model as geometrical parameters, and executed simulations for different stencil foil thicknesses (75–175 μm). Based on the computer simulation results, the necessary distance in the level difference range of 0–60 μm to get the stencil be able to bend down to the soldering pads is: $1.6 \cdot d \cdot h$ (d – stencil foil thickness, h – level difference). Considering the boundary conditions of the simulations the greatest minimum distance for a 90 μm level difference paired with a 175 μm stencil foil thickness was calculated to 31 mm.

Corresponding results were published in: R2

Applicability of the results

The measurement method presented in **Thesis I/1**, was developed for the order of Continental Temic Hungary Ltd. Using my measurement method to characterize the quality of solder joints of surface mounted resistors, this manufacturing company was able to control its manufacturing process more precisely. The supervisors can interact into the manufacturing process in the case of any (even tiny) failures immediately.

Based on the results of **Thesis I/2**, the electronics manufacturing companies can define a threshold for the acceptable position offset of small surface mounted components after soldering, by taking into account the permitted shear strength level of the solder joints of given components. The widely used threshold is the 80% of the optimal value of the shear strength.

The scientific benefit of **Part I** is that the results achieved by any experiments for examining the mechanical properties of solder joints of surface mounted passive discrete component of any sizes become directly comparable by the application of my method.

Using the results of **Part II** the electronics manufacturing companies can define a threshold for the position offset of components before soldering knowing that for example in what extent the components of size code 0603 are able to align to the right position during reflow soldering. The results were also applied directly in the successfully closed FP6 project called Leadout in which project the task was the adaptation of the lead free soldering technologies.

The results of **Part III** are applied by the German electronics manufacturing company called Bosch. The minimum technological distance which should have between the soldering surfaces of fine-pitch surface mounted electronic components and the pattern causing the level differences on the bare board is already added to the guidelines applied during the design of the circuit boards. Furthermore if this distance cannot be held because of the high integrity of the electronic circuits, the extent of the required decreasing of the volume of the stencil aperture can also be defined based on the results of Part III.

List of publications

The list of publications corresponding to thesis

Papers published in reviewed international journals in English

- [L1] **O. Krammer**, B. Sinkovics: „Improved method for determining the shear strength of chip component solder joints”, *Microelectronics Reliability*, Vol. 50, Issue 2, 2010. february, pp. 235-241.

Papers published in reviewed Hungarian journals in English

- [L2] **O. Krammer**, Zs. Illyefalvi-Vitéz: „Investigating the Self-alignment of Chip Components during Reflow Soldering”, *Periodica Polytechnika- Electrical Engineering*, Vol. 52 (2008), Issue 1-2, pp. 67-75.

Papers published in referenced proceedings of international conferences in English

- [R1] **O. Krammer**, L.M. Molnar, L. Jakab, C. Klein: ”Investigating the Increment of Deposited Solder Paste due to Uneven PCB Surface”, *33rd International Spring Seminar on Electronics Technology, IEEE-ISSE2010*, Warsaw, Poland, 12.05.2010.-16.05.2010., pp. &-&.
- [R2] **O. Krammer**, L.M. Molnar, L. Jakab, C. Klein: ”Stencil Deformation during Stencil Printing”, *15th International Symposium for Design and Technology of Electronics, IEEE-SIITME2009*, Gyula, Hungary, 17.09.2009.-20.09.2009., pp. 179-184.
- [R3] **O. Krammer**, Z. Radvánszki, Zs. Illyefalvi-Vitéz: „Investigating the Movement of Chip Components during Reflow Soldering”, *2nd Electronics Systemintegration Technology Conference, IEEE-ESTC2008*, Greenwich, England, 01.09.2008.-04.09.2008., pp. 851-856.
- [R4] **O. Krammer**, B. Sinkovics, B. Illés: „Studying the Dynamic Behaviour of Chip Components during Reflow Soldering”, *30th International Spring Seminar on Elctronics Technology, IEEE-ISSE2007*, Cluj-Napoca, Romania, 09.05.2007.-13.05.2007., pp. 18-23.
- [R5] **O. Krammer**, B. Sinkovics, B. Illés: „Predicting Component Self-Alignment in Lead-Free Reflow Soldering Technology by Virtue of Force Model”, *1st Electronics Systemintegration Technology Conference, IEEE-ESTC2006*, Dresden, Germany, 05.09.2006.-07.09.2006., pp. 617-623.

Papers published in proceedings of international conferences in English

- [K1] **O. Krammer**, Zs. Illyefalvi-Vitéz: „Investigating the shear strength of chip component solder joints”, *14th International Symposium for Design and Technology of Electronic Package, SIITME2008*, Brasov, Romania, 18.09.2008.-21.09.2008., pp. 301-305.
- [K2] **O. Krammer**, B. Sinkovics: „Investigation of the influence of surface mounted chip component misalignment on solder joint reliability”, *International microelectronics and packaging conference, IMAPS2007*, Rzeszow, Poland, 23.09.2007.-26.09.2007., pp. &-&.

Other publications

Book chapters

- [T1] B. Balogh, R. Berényi, L. Gál, P. Gordon, I. Hajdú, G. Harsányi, B. Illés, Zs. Illyefalvi-Vitéz, **O. Krammer**, J. Pinkola: „Elektronikai Technológia Laboratórium - Segédlet az Elektronikai technológia (BMEVIETA302) tárgyhoz”, IN: 55082, 2007, p. 40.
- [T2] B. Balogh, R. Berényi, L. Gál, P. Gordon, I. Hajdú, G. Harsányi, B. Illés, Zs. Illyefalvi-Vitéz, **O. Krammer**, J. Pinkola: „Electronics Technology Laboratories-Syllabus for Electronics Technology (BMEVIETA302), Identification number: 55083, 2007, p. 40.

Papers published in reviewed international journals in English

- [L3] B. Sinkovics, **O. Krammer**: „Board level investigation of BGA solder joint deformation strength”, *Microelectronics Reliability*, Vol. 49, Issue 6, 2009. June, pp. 573-578.

Papers published in Hungarian journals in English

- [L4] M. Janóczki, Z. Radvánszki, L. Jakab, **O. Krammer**: „X-ray Imaging in Pin-in-Paste Technology”, *Periodica Polytechnica- Electrical Engineering*, Vol. 52 (2008), Issue 1-2, pp. 21-29.

Papers published in referenced proceedings of international conferences in English

- [R6] **O. Krammer**, I. Kobolák, L.M. Molnár: „Method for selective solder paste application for BGA rework”, *31st International Spring Seminar on Electronics Technology, IEEE-ISSE2008*, Budapest, Hungary, 07.05.2008.-11.05.2008., pp. 432-436.

- [R7] B. Illés B, **O. Krammer**, G. Harsányi, Zs. Illyefalvi-Vitéz, A. Szabó: „3D Investigations of the Internal Convection Coefficient and Homogeneity in Reflow Ovens”, *30th International Spring Seminar on Electronics Technology, IEEE-ISSE2007*, Cluj-Napoca, Romania, 09.05.2007.-13.05.2007., pp. 320-325.
- [R8] **O. Krammer**, B. Illés: „Lead-Free Soldering Technology Review - Evaluating Solder Pastes and Stencils”, *29th International Spring Seminar on Electronics Technology, IEEE-ISSE2006*, St. Marienthal, Germany, 10.05.2006.-14.05.2006., pp. 86-91.
- [R9] Zs. Illyefalvi-Vitéz, **O. Krammer**, J. Pinkola: „Testing the Impact of Pb-free Soldering on Reliability”, *1st Electronics Systemintegration Technology Conference, IEEE-ESTC2006*, Dresden, Germany, 05.09.2006.-07.09.2006., pp. 468-472.
- [R10] B. Illés, **O. Krammer**, G. Harsányi, Zs. Illyefalvi-Vitéz: „Modelling Heat Transfer Efficiency in Forced Convection Reflow Ovens”, *29th International Spring Seminar on Electronics Technology, IEEE-ISSE2006*, St. Marienthal, Németország, 10.05.2006.-14.05.2006., pp. 80-85.
- [R11] B. Illés, **O. Krammer**, G. Harsányi, Zs. Illyefalvi-Vitéz, A. Szabó: „Effect of Component-Level Heat Conduction on Reflow Soldering Failures”, *1st Electronics Systemintegration Technology Conference, IEEE-ESTC2006*, Dresden, Germany, 05.09.2006.-07.09.2006., pp. 1386-1392.
- [R12] I. Hajdu, Zs. Kincses, **O. Krammer**: „Noise study method of soldering joints”, *29th International Spring Seminar on Electronics Technology, IEEE-ISSE2006*, St. Marienthal, Germany, 10.05.2006.-14.05.2006., pp. 296-298.
- [R13] **O. Krammer**: „The Effect of Lead-free Soldering on Formation of Black Pad Failure”, *28th International Spring Seminar on Electronics Technology, IEEE-ISSE2005*, Wiener Neustadt, Austria, 19.05.2005.-20.05.2005., pp. 191-195.

Papers published in proceedings of international conferences in English

- [K3] B. Sinkovics, **O. Krammer**, L. Jakab: „Experimental and numerical analysis of mechanical behavior of multilayer PWB assemblies”, *14th International Symposium for Design and Technology of Electronic Package, SIITME2008*, Brasov, Romania, 18.09.2008.-21.09.2008., pp. 345-349.
- [K4] **O. Krammer**, B. Sinkovics, Zs. Illyefalvi-Vitéz, L. Jakab, A. Szabó: „Board level investigation of BGA solder joint deformation strength”, *International microelectronics and packaging conference, IMAPS2008*, Pułtusk, Poland, 21.09.2008.-24.09.2008., Paper 34., pp. &-&.
- [K5] Zs. Illyefalvi-Vitéz, L. Gál, **O. Krammer**, J. Pinkola: „Via Fabrication Techniques for High Density Vertical Interconnections”, *16th European Microelectronics and Packaging Conference EMPC2007*, Oulu, Finland, 15.06.2007.-17.06.2007., pp. 660-665.

- [K6] **O. Krammer**, A. Nyakó, B. Illés: „Measuring Methods of Solder Paste Hole Filling in Pin-in-Paste Technology”, *13th International Symposium for Design and Technology of Electronic Package, SIITME2007*, Baia Mare, Romania, 20.09.2007.-23.09.2007., pp. 146-150.
- [K7] Zs. Illyefalvi-Vitéz, **O. Krammer**, R. Bátorfi: „Experimental Life-time Prediction of Pb-free Solder Joints”, *13th International Symposium for Design and Technology of Electronic Package, SIITME2007*, Baia Mare, Romania, 20.09.2007.-23.09.2007., pp. 115-118.
- [K8] Zs. Illyefalvi-Vitéz, P. Németh, **O. Krammer**, J. Pinkola: „Comparison of Accelerated Life-time Test Methods of Pb-free Solder Joints”, *16th European Microelectronics and Packaging Conference, EMPC2007*, Oulu, Finland, 10.06.2007.-12.06.2007., pp. 419-424.
- [K9] B. Illés, **O. Krammer**: „Variation of Gas Flow Parameters in Forced Convection Reflow Oven”, *13th International Symposium for Design and Technology of Electronic Package, SIITME2007*, Baia Mare, Romania, 20.09.2007.-23.09.2007., pp. 27-31.
- [K10] **O. Krammer**, B. Illés: „Comparative Study of Stencils for Advanced Lead-Free Reflow Soldering Technologies”, *12th International Symposium for Design and Technology of Electronic Package, SIITME2006*, Iasi, Romania, 21.09.2006.-24.09.2006., pp. 58-62.
- [K11] Zs. Illyefalvi-Vitéz, **O. Krammer**, J. Pinkola: „Soldering and Reliability Trials using Pb-free Solders”, *12th International Symposium for Design and Technology of Electronic Package, SIITME2006*, Iasi, Romania, 21.09.2006.-24.09.2006., pp. 44-48.
- [K12] Zs. Illyefalvi-Vitéz, **O. Krammer**, J. Pinkola, B. Riegel, N. Ruzsics, G. Juhász: „Lead-free Soldering Implementation Issues”, *4th European Microelectronics and Packaging Symposium, EMPS2006*, Terme Catez, Slovenia, 21.05.2006.-24.05.2006., pp. 231-236.
- [K13] B. Illés, **O. Krammer**, G. Harsányi, Zs. Illyefalvi-Vitéz, A. Szabó: „3D Thermodynamics Analysis Applied for Reflow Soldering Failure Prediction”, *4th European Microelectronics and Packaging Symposium, EMPS2006*, Terme Catez, Slovenia, 21.05.2006.-24.05.2006., pp. 217-222.
- [K14] **O. Krammer**, B. Illés: „Reflow Soldering Optimization in Lead-Free Environment: Immersion silver finishes are an alternative for Electroless Nickel Immersion Gold finishes”, *11th International Symposium for Design and Technology of Electronic Packages, SIITME2005*, Cluj-Napoca, Romania, 22.09.2005.-25.09.2005., pp. 85-89.

Other papers published in Hungarian journals

- [M1] **Krammer O.**: „Az ólommentes forrasztás hatása a Black Pad kialakulására”, *Elektronet*, 2005. September, pp. 57-60.

References

- [1] K.S. Kim, S.H. Huh, K. Suganuma: „Effects of fourth alloying additive on microstructures and tensile properties of Sn–Ag–Cu alloy and joints with Cu”, *Microelectronics Reliability*, Vol. 43 (2003), pp. 259–267.
- [2] M.N. Islam, Y.C. Chan, A. Sharif, M.O. Alam: „Comparative study of the dissolution kinetics of electrolytic Ni and electroless Ni–P by the molten Sn_{3.5}Ag_{0.5}Cu solder alloy”, *Microelectronics Reliability*, Vol. 43 (2003), pp. 2031–2037.
- [3] Ming-Chih Yew, Chan-Yen Chou, Kuo-Ning Chiang: „Reliability assessment for solders with a stress buffer layer using ball shear strength test and board-level finite element analysis”, *Microelectronics Reliability*, Vol. 47 (2007), pp. 1658–1662.
- [4] G.Y. Li and Y. C. Chan: „Aging Effects on Shear Fatigue Life and Shear Strength of Soldered Thick Film Joints” *IEEE Transaction on Components, Packaging, and Manufacturing Technology—Part B*, Vol. 21, No. 4, 1998. november, pp. 398–406.
- [5] K.S. Kim, S.H. Huh, K. Suganuma: “Effects of intermetallic compounds on properties of Sn–Ag–Cu lead-free soldered joints”, *Journal of Alloys and Compounds*, Vol. 352 (2003), pp. 226–236.
- [6] R. Wassink, M. Verguld: „Drawbridging of leadless components”, *Hybrid Circuits*, No. 9, 1986. january, pp. 18–24.
- [7] J.R. Ellis, G.Y. Masada: „Dynamic Behavior of SMT Chip Capacitors During Solder Reflow”, *IEEE Transaction on Components, Hybrids, and Manufacturing Technology*, Vol. 13, No. 3, 1990. september, pp. 545–552.
- [8] Y. Zhang, R. Zhao, D.K. Harris, R.W Johnson: „A Computational Study on Solder Bump Geometry, Normal, Restoring, and Fillet Forces During Solder Reflow in the Presence of Liquefied Underfill”, *IEEE Transaction on Electronics Packaging Manufacturing*, Vol. 25, No. 4, 2002. oktober, pp. 308–317.
- [9] L. Hua, C. Bailey: „Dynamic Analysis of Flip-Chip Self-Alignment”, *IEEE Transaction on Advanced Packaging*, Vol. 28, No. 3, 2005. augustus, pp. 475–480.
- [10] R.W. Kay, S. Stoyanov, G.P. Glinski, C. Bailey, M.P.Y. Desmulliez: „Ultra-Fine Pitch Stencil Printing for a Low Cost and Low Temperature Flip-Chip Assembly Process”, *IEEE Transactions on Components and Packaging Technologies*, Vol. 30, No. 1, 2007. march, pp. 129–136.
- [11] S.H. Mannan, N.N. Ekere, E.K. Lo, I. Ismail: „Predicting Scooping and Skipping in Solder Paste Printing for Reflow Soldering of SMT Devices” *Soldering & Surface Mount Technology*, Vol. 5, Issue 3, 1993, pp. 14–17.
- [12] R. Durairaj, S. Ramesh, S. Mallik, A. Seman, N. Ekere: „Rheological characterisation and printing performance of Sn/Ag/Cu solder pastes” *Materials and Design*, Vol. 30 (2009), pp. 3812–3818.