

RECEIVER SYNCHRONIZATION FOR 2-FSK COMMUNICATION SYSTEMS

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I. Introduction

In this paper a robust and effective synchronization technique is presented for a low transmit data rate communication using frequency shift keying (2-FSK). Due to security purposes the designed system has to be very stable with low packet error rate and should be capable to operate at low signal to noise ratios (SNR).

The main idea of digital communication systems is to transmit binary information through the medium. A schematic block diagram of a digital communication system is shown in Fig.1. First the the bitstream is mapped to baseband analog signal. Then the carrier signal is modulated by the baseband signal and transmitted after a high power amplifier (HPA) trough the medium. Depending on which parameter of the carrier wave is manipulated, we can talk about amplitude, phase or frequency modulation [1]. At the receiver we use first apply a low noise amplifier, the other steps are the inverse of the above described steps. The baseband signal processing blocks (shaded blocks) will be the main topic in this paper. Although it is not shown in the figure, a key issue is the synchronization of

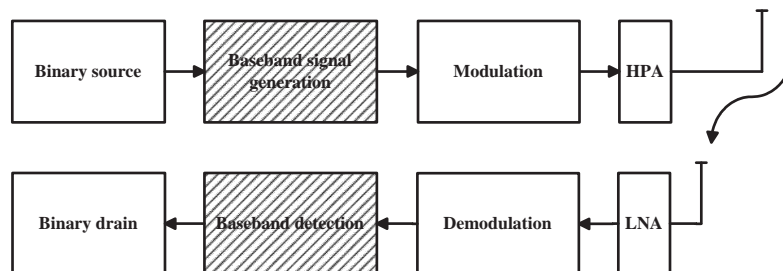


Figure 1: Block diagram of simplified digital communication system

the received signal at the receiver. Timing, phase and frequency synchronization must be performed to retrieve the correct data [2]. In this paper we will show a synchronization method for a simple system using frequency shift keying (FSK) in the baseband. Modulation in our case means a simple up-converting to the desired transmit channel.

As baseband signalling we use frequency shift keying (FSK). A 2-FSK system transmits one bit at time over a symbol length T_s , using 2 frequencies f_1 and f_2 with the following elementary analog symbols:

$$\begin{aligned} s_1(t) &= \sin(2\pi f_1 t), & 0 < t < T_s, & \text{ representing bit "0"} \\ s_2(t) &= \sin(2\pi f_2 t), & 0 < t < T_s, & \text{ representing bit "1"} \end{aligned}$$

The frequency shift keying modulation is one of the most robust modulation techniques, therefore this is one of the best choices for transmitting in a noisy channel. In our case the baseband frequency bandwidth is 3600 Hz.

II. Structure of the baseband transmission signal

To comply with the international standards we chose the following 2 frequency values for the elementary symbols: 1200 Hz and 2400 Hz. It is also important to mention that a data rate of 2400 bps had to be achieved, so a total period of the 2400 Hz signal is applied and a half period of the 1200 Hz signal. To keep the signal continuity between consecutive elementary symbols, we also use the inverted versions of the elementary symbols for transmission. A transmission signal is constructed from these major parts:

- Due to the properties of the receiver, for a certain time a signal has to be transmitted to open the squelch of the receiver radio (Squelch).
- A synchronization pattern has to be transmitted so the symbol borders can be extrapolated (Synchronization bytes). This pattern is a continuous alternation between the two elementary symbols.
- A given bit pattern has to signal the beginning of the packet (Flag). The flag pattern is 01111110.
- The packet contains the data bits (Packet). It is important that it does not contain any flag pattern, this can be eliminated by bitstuffing (after every fifth 1 bit a 0 is inserted).
- A given bit pattern has to signal also the end of the packet (Flag).

An example for a transmission signal – with all the above described properties – is visualized in Fig. 2. Also the inverted elementary symbols for keeping the time domain continuity can be observed.

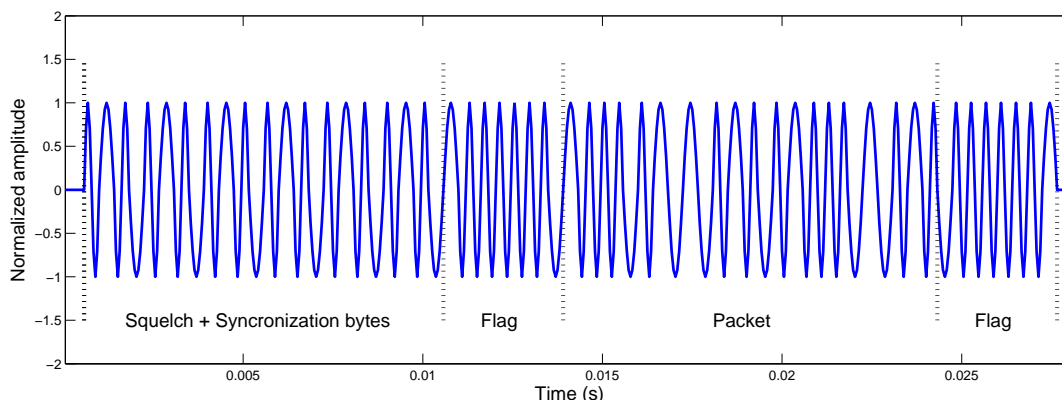


Figure 2: Structure of the baseband transmission signal

III. The synchronization and demodulation algorithm

A. Correlation principle

The receiver has to perform the synchronization based on the samples taken from the received signal. The synchronization algorithm is based on the correlation principle [3]. The discrete cross correlation between the incoming signal and the ideal elementary symbols has to be calculated. The two elementary symbols are orthogonal to each other for the symbol length:

$$\int_0^{T_s} s_1(t)s_2(t) = 0.$$

In the discrete case, where we have N samples from a symbol, we obtain: $\sum_0^{N-1} s_1[k]s_2[k]$. The receiver algorithm will take advantage of this property to decide between the two symbols.

B. The synchronization algorithm

The block diagram of the receiver structure with the synchronization algorithm is depicted in Fig. 3. First, a sample is taken from the incoming baseband analog signal. In general $N = 2^m$ samples are

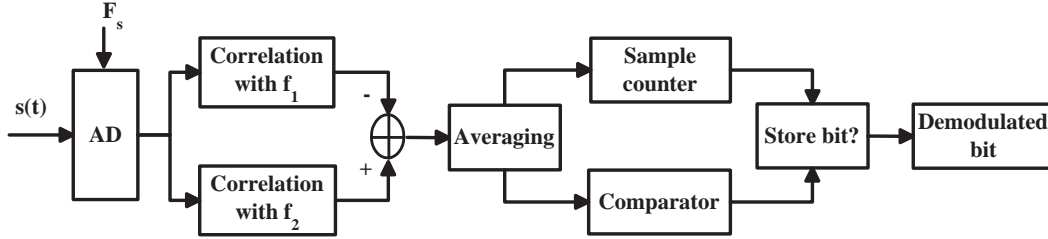


Figure 3: Block diagram of the receiver and synchronization algorithm

taken from one symbol length T_s , so the sampling frequency is equal to $F_s = N * 2400$ Hz. Then a filtering – in other words, a cross correlation calculation with s_1 and s_2 and with their cosine versions – is performed between the incoming samples and the ideal ones. In the next step the difference of the two correlation results is calculated. With some restrictions it can be also interpreted as an N point Fourier transform [4] for two frequency values, and the difference between the two amplitude values is formed. This difference is then averaged to suppress the effect of noise.

The sample counter can have the values of $0 \dots N-1$. If the sample counter reaches $N - 1$, a decision can be performed. If the sign of the output of the averaging filter block is changing, we can assume that we are at the half of a symbol length, so we can set our sample counter to $N/2$. On the other hand, if the absolute value of the output is smaller than a threshold – this threshold for the noise was determined by simulations –, then we can assume that we did not receive any signal, only noise, so we don't have to make any decisions. The sign of the averaging filter determines the demodulated bit, if it is negative, than we have a 0 bit, otherwise a 1 bit is received. After each decision the sample counter value is set back to 0.

Due to averaging, we will have a delay of one symbol length between the decision and the current incoming symbol. Synchronization of the symbol borders are done in every case when there is a change in the bits, due to the fact that averaging changes its sign, so the sample counter is set to the correct value.

If only 0 bits are transmitted, it will demodulate but in case of sampling time differences it can lead to loss of bits, due to the fact that no changes are inside the packet, so no sample counter correction is performed. This problem can be eliminated by introducing an extra NRZ (Non Return to Zero) coding to the bitstream inside the packet. Another drawback of this synchronization principle is that it is sensitive to small amplitude offsets, because the correlation with the s_0 symbol will provide a small value, but the correlation with s_1 totally eliminates it. To improve the algorithm, the number of samples N taken from the incoming signal can be increased, although it is important to execute the synchronization algorithm between two sampling instants.

The output of the averaging filter for a signal to noise ratio of 10 dB is shown in Fig. 4. It can be seen that if only noise is present it has no influence on the detection, although decisions are made, but due to the fact that the values are under the decision threshold these are neglected. The two flags – packet start and packet end – can be also recognized. The receiver recovers the transmitted data for the received signal without errors. The normalized output of the averaging filter is set so, that without noise it reaches only 75% of the maximum value (maximum value is show with dashed lines at 1 and -1), this will lead to a margin for the noise effects. The threshold for the noise is shown by 2 dotted lines at the value 0.125.

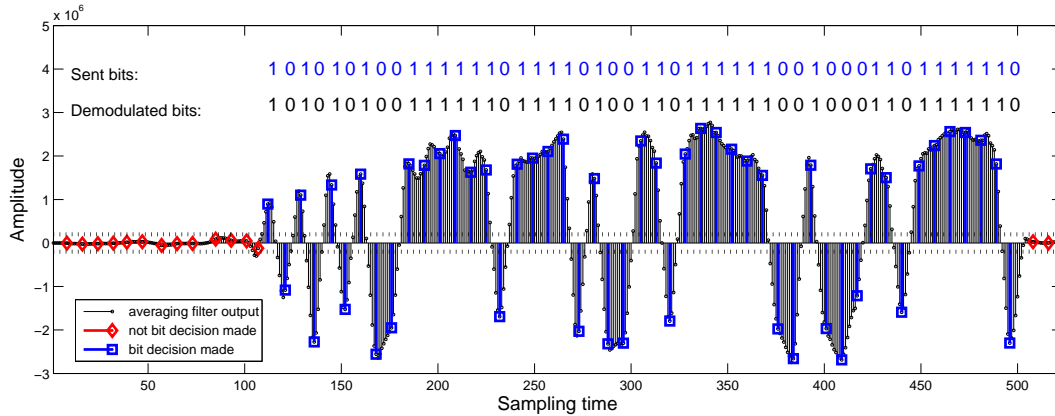


Figure 4: Output of the averaging block with decisions

C. Demodulation algorithm

If the algorithm achieves synchronization it begins to demodulate the received bits. The incoming bits are stored until the packet start pattern is found: 01111110_2 . Then, the algorithm stores the incoming bits until the closing pattern is found. After the closing flag arrives, the packet is processed.

IV. Conclusion

We have described robust synchronization algorithm for 2-FSK system. We have approved with simulation that it is effective if the SNR ratio is higher than 5 dB, and we have also shown that it is not severely affected by small timing offsets. The above described algorithm is also implemented and tested in DSP.

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