



Budapest University of Technology and Economics  
Faculty of Electrical Engineering and Informatics

# New method for functional-thermal co-simulation of integrated circuits

Ph.D. Thesis Booklet

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Budapest, 2019.

# 1 Introduction

In the past one and a half decade, the evolution of integrated circuits' performance became limited by the increasing dissipation density that led to thermal related issues (Figure 1).

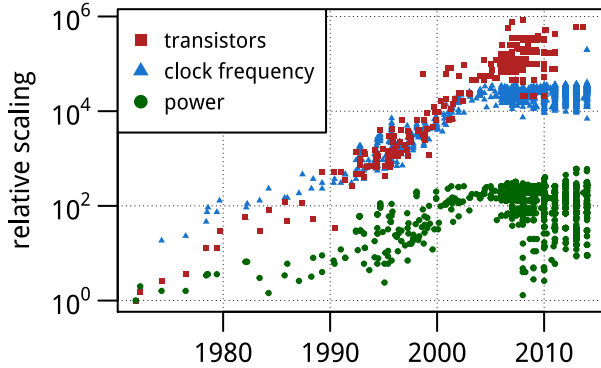


Figure 1: Scaling of the processors' parameters between 1970 and 2014

To overcome this issue, the manufacturers are developing better cooling solutions and advanced controlling schemes, which monitor the utilization and the temperature of the IC die at different locations. As long as the fundamental structure of mainstream semiconductor devices do not change, the behavior of high-end integrated circuits will be strongly influenced by the thermal environment. This issue prompts that the effect of the die's temperature on the integrated circuits' functional behaviour should be taken into account, preferably early in the design flow.

## Previous work

At the Department of Electron Devices in the Budapest University of Technology and Economics, Kálmán Tarnay and Vladimír Székely worked first in the field of integrated circuits' electrical/functional and thermal co-simulation. Their work grounded the research work of my colleagues, László Pohl, András Timár and Gergely Nagy. I started my research based on their work. The kickoff of the logi-thermal simulation in the department's thermal research group is an IEEE article published in 1997 [1].

Based on the logi-thermal simulation paradigm [1], András Timár implemented a co-simulation framework using standard EDA tools. The new simulation framework could consider the standard cells' temperature-dependent delays [2]. Gergely Nagy improved the method further by developing a unique logic simulator engine and integrated it with an in-house thermal simulator [3].

Other research groups also aimed to join the thermal and functional modeling. T. Bouhadiba's work can be used to analyze the thermal and functional behavior of high-level models [4]. S. Vinco's research utilizes SystemC to connect the different simulation domains. Intra- and interdomain communication is realized by the SystemC and SystemC-AMS languages, which are also used for modelling purposes. The Ctherm functional-thermal simulator uses the IP components of an open platform library for functional models, and the widely known HotSpot for thermal simulations [5]. Similarly, M. y. Hsieh extended an open source simulator package with dissipation, thermal, and reliability modeling components [6].

The common denominator in the above solutions is that they are restricted to a single abstraction level, i.e. they can work only on gate level or high abstraction level.

## **Research aims and objectives**

During my research, I focused on the simulation of the integrated circuits' temperature dependent behavior. The objective of my work was to create a simulation methodology that does not have the limitations of the approaches mentioned above, i.e. it can be used for circuits implemented on arbitrary abstraction level, and it can simulate the temperature dependent behavior with acceptable accuracy on that specific level of abstraction. The general applicability was high priority during the elaboration of the new methodology, which is ensured by its integration into the standard design flow. This can be achieved, if the extra information needed by the new method is available on the required abstraction level.

## 2 Applied tools and inspection methodologies

In accordance with the goal set in the first phase of the research, during the elaboration of the new simulation methodology I used standard tools, i.e. the modeling languages, simulators, and additional IC EDA tools are all used in conventional design flows. The demonstrator circuits were implemented in SystemC, SystemC-AMS, and Verilog languages. Digital and mixed-signal simulations were performed with SystemC, Mentor<sup>®</sup> Questa<sup>™</sup> Sim and Cadence<sup>®</sup> IES, and analog circuits were simulated with Cadence<sup>®</sup> Virtuoso<sup>®</sup>. RTL and physical synthesis were performed using Cadence<sup>®</sup> RTL Compiler and Encounter<sup>™</sup>, the target technology was AustriaMicroSystems' 0,35  $\mu\text{m}$  CMOS standard cell library. Layout specified in LEF/DEF format, and the PDK's Liberty<sup>™</sup> database were imported by open source software. Additionally I also used the Sniper x86 processor simulator [7] to demonstrate the capability of the new co-simulation methodology.

In contrast with the standard tools used for functional modeling of integrated circuits, thermal simulation solutions are adopted in a narrower range. The IC designer companies will use the CAD tools for thermal simulation, which suits best for their requirements. Additionally several academic simulator exist for thermal simulation of IC dies. During my research I used simulators from the latter category, the successive network reduction algorithm based SUNRED [8], the open souce 3D-ICE [9], and HotSpot [10] simulators can model the thermal environment of an integrated circuit. I also developed a thermal simulator, which utilizes the PARALUTION linear algebra library [11] for solving the thermal equations.

Based on my research results, I implemented a co-simulation framework in C++ and Python programming languages, the processing and visualization of the simulation results were performed by R scripts.

### 3 New scientific results

#### Abstract interface

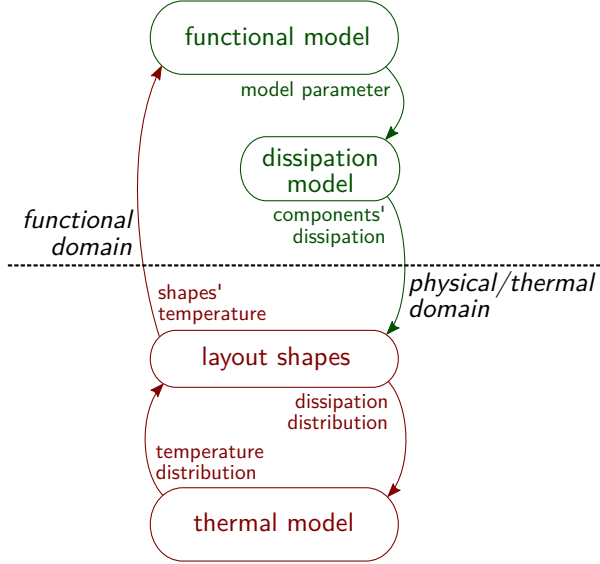


Figure 2: Relaxation co-simulation method realized by the interface

To connect the functional ( $F$ ) and thermal ( $T$ ) domains, I introduced the terms *functional model component* ( $F_i$ ), *dissipation source* ( $p_i$ ) and *layout shape* ( $L_i$ ).

**Functional model component** The  $F_i$  functional model components are the disjunct sets of the functional model, the temperature of such component is described by its  $T_i$  parameter.

**Dissipation source** The dissipation sources are elements of the  $P$  dissipation model. One  $p_i$  dissipation source can be assigned to every  $F_i$  functional model component, which determines the power dissipation of that component.

**Layout shape** The layout arrangement is the part of the  $T$  thermal model. The layout consists of  $l_{ij}$  rectangles, which have  $\{x, y, z\}_p$  position and  $\{x, y\}_a$  size. Based on these information, the temperature of the layout primitives can be determined. The union of the rectangles are one  $L_i$  layout shape, which can be assigned to one  $F_i$  functional model component. Every pair of layout shape is disjunct.

**Thesis I** *I have developed an abstract interface connecting the functional and thermal domains of integrated circuit models. The new interface can be used by relaxation based functional-thermal co-simulation methods, and it can be attached to simulators using arbitrary modeling languages and abstraction levels [J1, J2, J3],[C1, C2, C3].*

## Extended design flow

To use the new simulation method described in Thesis I for real-life designs, the representation of the abstract interface's elements must be realised for the required abstraction level. During development, the functional model is usually implemented in a hardware modeling language. The functional model consists of components, which can be organized in a hierarchy. These components may contain concurrent statements and sequential blocks as well. In the conventional EDA tools – such as RTL/logic synthesis tools – the hierarchical component is the smallest element that can be identified unambiguously.

To preserve the generic nature of the method defined in Thesis I, the hierarchical components of the HDL languages were chosen as functional model components  $F_i$ . Conventional EDA tools – such as high level, RTL/logic or physical synthesis tools, or other modeling approaches from the literature can be used to generate the  $p_i$  dissipation source and  $L_i$  layout shape as long as they can be fitted to functional

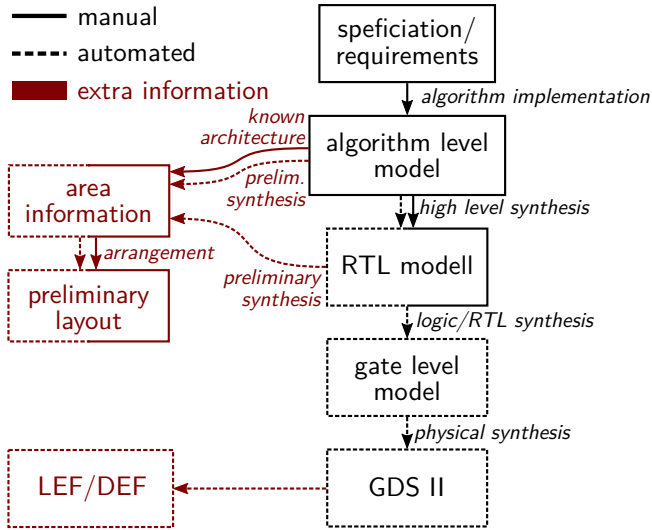


Figure 3: Method for constructing the layout arrangement

models implemented in standard hardware modeling languages (Figure 3 and 4).

In case of gate level, the new simulation method corresponds with the logi-thermal simulation realized by Timár András [2]. Based on the functional description containing instances of standard cells, a dissipation source and layout shape can be assigned to every logic gate. Based on the switching activity registered in the logic simulator kernel and the energy dissipation values stored in the *Liberty* database, the power dissipation can be calculated and sent to the thermal simulator engine. The size and position of the layout shapes can be determined from the physical synthesis tool in LEF/DEF format.

On register transfer level, the exact physical implementation of the circuit is not available. Many research article addressed the issue of RTL dissipation modeling, thus an estimation can be applied. If a given dissipation model can be generated/characterized and attached

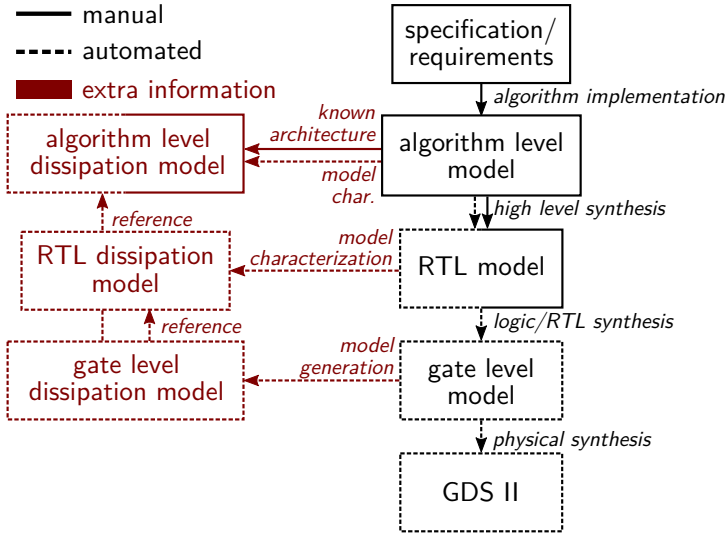


Figure 4: Method for constructing the dissipation model

to standard EDA tools, it can be used in the extended design flow for functional-thermal simulation. The size and position of layout shapes can be estimated using a preliminary synthesis result. One dissipation source and layout shape can be assigned to one functional model component. This restriction is the result of the limitation of current EDA tools, as the modules/entities are the smallest elements that can be identified across different levels of abstraction.

The thermal resolution is determined by the number of different modules/entities. To achieve better results, it is recommended to partition the design into smaller different modules/entities. Beside the functional behavior, structural RTL models contain more information about the structure of the circuit. This coding style is favored for functional-thermal simulation, as the RTL model will consist of smaller functional modules/entities.

Multiple linear regression dissipation models can be used for power dissipation estimation for these types of RTL descriptions [12]. The dissipation estimated by the dissipation source is determined by the switching activity of the module's/entitie's ports. This method is applicable if the module's internal activity is also displayed on the activity of its ports.

**Thesis II** *I have developed a method to extend the conventional design flow of integrated circuits by functional-thermal simulation using the interface described in Thesis I. In the extended design flow, any dissipation source and layout shape models can be used, which are introduced in the literature, if they can be accommodated by the formal languages and functional simulator tools used in the regular design flows, or they can be connected to the unique simulator fitted to the interface. This solution can be used to analyze the thermal behavior of the circuit in the same thermal environment in different phases of the design flow [J1, J2], [C4].*

## New thermal simulator

During thermal simulation, different time-steps should be applied to track fast thermal transients, and near steady state temperatures. At the beginning of a transient, the temperature changes in a greater extent, thus the equation system modeling the thermal problem must be evaluated in shorter time periods. Applying increasing time-steps in logarithmic scale is common practice for thermal simulation and measurement, as the response for step change stimuli is an exponential curve. This approach cannot be used for functional-thermal simulation, as the stimuli changes over time, its future value is unknown.

The TRANZ-TRAN electro-thermal simulation uses direct co-simulation method to solve the multi-domain equation system. It uses an adaptive algorithm, which can change the simulation's time-step if

required [13]. If the time-step is too large, it is possible that the solver does not converge to the accurate solution, but finds a different local minimum. In a situation like this, TRANZ-TRAN disposes the calculated result, reduces the simulation time-step, and solves the equations again from a randomly selected point.

Other common method to connect multiple simulation domains is the relaxation approach. The data exchange rate between the different simulator engines is important as the functional simulator assumes constant temperatures during two consecutive thermal simulations. If the co-simulation time-step is too large, the temperatures can change in a greater extent during the following thermal simulation resulting inaccurate results. This problem can be eliminated if the co-simulation timestep is smaller, than the layout shapes' ( $L_i$ ) smallest thermal time constant.

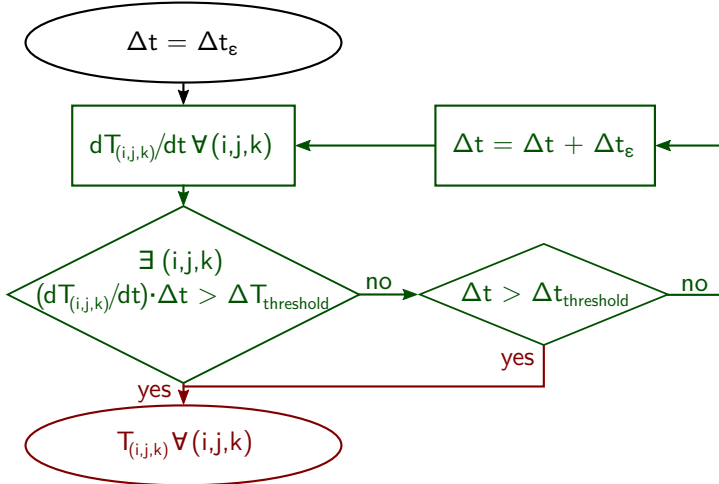


Figure 5: Adaptive algorithm for determining time-step

Due to the above mentioned reasons, I have implemented an algorithm, which can estimate the temperature change based on the time derivative of the temperature and the elapsed time since the

last thermal simulation (Figure 5). The algorithm is evaluated in  $t_e$  time-steps. The  $\Delta t$  variable stores the elapsed time since the last thermal simulation,  $\Delta T_{\text{threshold}}$  and  $\Delta t_{\text{threshold}}$  variables are inputs of the algorithm. The first parameter is the temperature threshold. If the estimated temperature change is larger than this constant, the new temperature values are calculated by the solver. The second parameter is the maximum allowed time-step. If  $\Delta t$  reaches this value, the equation system will be solved. The algorithm uses forward Euler method to estimate the temperature change, thus the real change will always be smaller.

I performed three simulations of the same structure using constant 1 ms and 1  $\mu\text{s}$  time-steps, and adaptive time-step between 1  $\mu\text{s}$  and 1 ms. Table 1 shows the runtime and the error compared to the reference 1  $\mu\text{s}$  case.

<b>Time-step</b>	<b>Runtime</b>	<b>Error</b>
1 $\mu\text{s}$	8,77 h	
1 $\mu\text{s}$ – 1 ms	1,32 h	0,167 °C
1 ms	5,53 min	0,82 °C

Table 1: Comparison of runtime and error

Using constant 1 ms time-step the simulation is extremely fast, but large temperature changes can lead to error during functional-thermal co-simulation if the transient of the functional-thermal effect is shorter than the time-step. Using constant 1  $\mu\text{s}$  time-step, the temperature difference is small in consecutive thermal simulations, but the runtime is increased by a factor of 100. The adaptive approach has the advantage, that it can automatically change the time-step so it fits the stimuli and the system’s response most.

**Thesis III** *I have developed a new thermal simulator, which can better utilize the performance of modern processor architectures compared to current solutions. The new thermal simulation engine estimates the temperature change based on the input stimuli, and adaptively changes the thermal simulation's time-step. This method makes it possible to track the large temperature change when the stimuli changes to better align to the small thermal time constants, while reduce the computational requirement near steady state by using larger time-step [C5].*

### Functional-thermal verification method

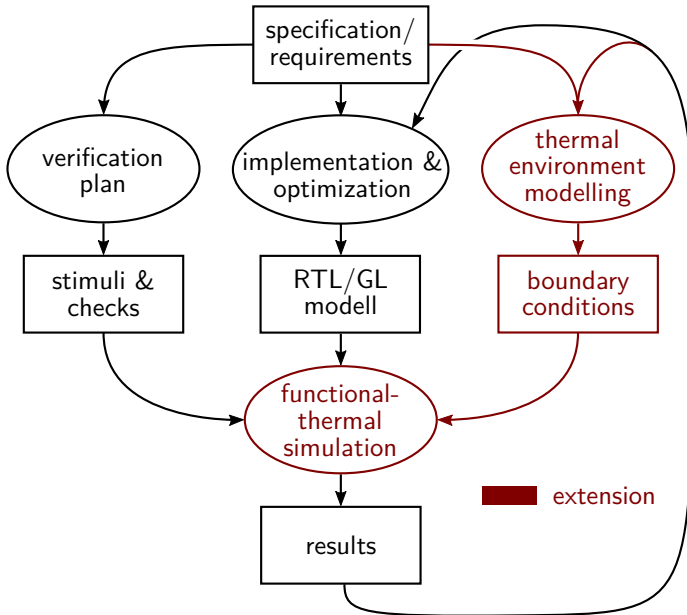


Figure 6: Functional-thermal verification process

Conventional verification process cannot take thermal effects into account, as the current modeling and simulator tools do not have thermal modeling capabilities. Functional-thermal verification is an extension of the regular functional verification. During functional-thermal verification, it is possible to model the circuits temperature dependent parameters and detect functional errors caused by the thermal environment.

Figure 6 illustrates the thermal aware functional verification process. In this verification process, the implementation of the functional model and the thermal environment modeling can occur in parallel. The thermal environment modeling task consists of creating the circuit's thermal model, modeling temperature dependent behavior and defining the boundary conditions.

## Simulation results

The capability of the functional-thermal verification process and the predictable errors are demonstrated with three processor systems implemented on different abstraction levels. The first system contains temperature dependent delay models of logic gates similarly to the work of András Timár. Compared to the CellTherm simulation framework implemented by him, the new co-simulation method is capable of simulating higher abstraction level models. Thus, only the critical path (with largest delay) must be realized on the level of logic gates, the rest of the processor can be modeled on register transfer level.

The runtimes of the two types of simulations differ in one order of magnitude, the simulation took 42 minutes in case of the mixed level model, and the gate level model simulation finished in 8 hour and 20 minutes. The relative error of the calculated delay was 2% compared to the reference gate level only logi-thermal simulation (Figure 7).

The second demonstration system realizes a PID control system using the a processor core, ADC, and DAC behavior models. As the DAC and ADC circuits' accuracy depends on the temperature, the

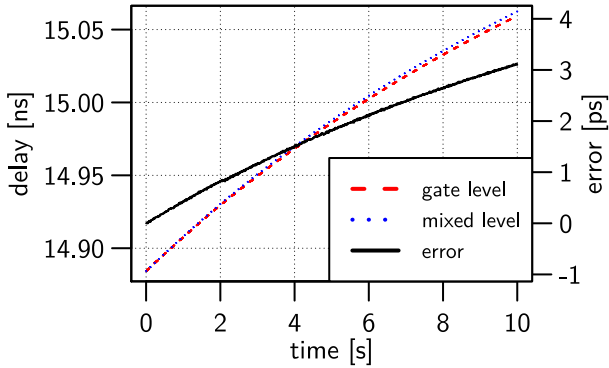


Figure 7: Delay of the critical path

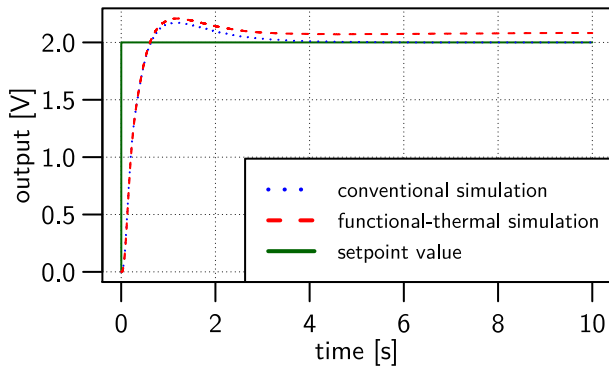


Figure 8: PID controller system's response to step change

response of the process to a step change in the setpoint had residual steady state error (Figure 8).

The third simulation uses a high abstraction level quad core x86 processor simulator model to analyze the behavior of a dynamic thermal management algorithm. The realized algorithm reduces a processor core's frequency if its temperature exceeds  $80^{\circ}\text{C}$  (Figure 9).

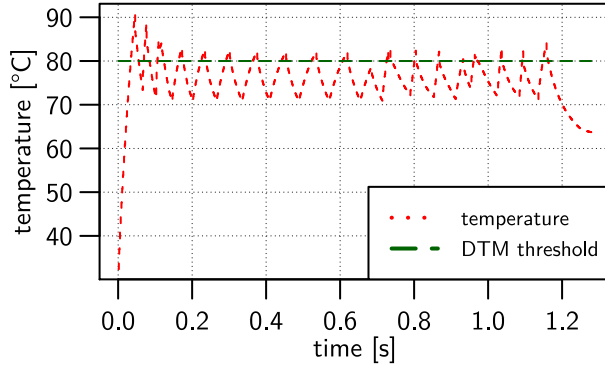


Figure 9: Temperature of the first core

**Thesis IV** *Based on the generic approach of the interface introduced in Thesis I, I have developed a method for functional-thermal verification of digital, analog and mixed-signal circuits. Temperature dependent parameters can also be considered during the new verification process, and beside the thermal environment of the circuit, conventional functional verification tools can be used [J2], [C6].*

## 4 Applications of the results

The functional-thermal simulation method based on the research results can be used in arbitrary step of the design flow to analyze the thermal behavior of integrated circuits. The mechanical and functional designs are related to the thermal restrictions. The effects of the two domains on each other should be simulated in the same simulation environment, which aids the work of the functional model's designers and the mechanical engineers working on the thermal solutions.

The new verification method can be used to support design decisions, which can effect the circuits thermal and functional behavior. It can be used to analyze different, temperature measurement based controlling methods, such as DTM or DVFS algorithms used in modern digital integrated circuits. This can only be achieved on transistor level by electro-thermal simulation tools available in conventional design flows.

## Journal Papers

- [J1] *L. Jani* and A. Poppe. Multilevel logic and thermal co-simulation. *Microelectronics Reliability*, 67:46–53, 2016. DOI:10.1016/j.microrel.2016.08.019.
- [J2] *L. Jani* and A. Poppe. Framework for thermal-aware verification of digital and mixed signal systems. *Microelectronics Reliability*, 68:1–12, 2017. DOI:10.1016/j.microrel.2017.03.023.
- [J3] M. Németh, G. Takács, *L. Jani*, and A. Poppe. Compact modeling approach for microchannel cooling and its validation. *Microsystem Technologies*, 23:1–13, 2017. DOI:10.1007/s00542-017-3330-z.

## Conference Proceedings

- [C1] *L. Jani* and A. Poppe. Extension of SystemC with logi-thermal simulation capabilities. In *International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, pages 1–4, Sept 2015. DOI:10.1109/THERMINIC.2015.7389604.
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*in Electronic Systems (ITHERM)*, pages 307–312, June 2017.  
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## Unrelated Publications

- [N1] *L. Jani* and *Z. Á. Mann*. Cache optimization for CPU-GPU heterogeneous processors. *American Journal of Algorithms and Computing*, 2(1):18–31, 2015. DOI:10.7726/ajac.2013.1001.
- [N2] *L. Jani* and *Z. Á. Mann*. Megosztott cache heterogén multiprocesszoros rendszerekben (1. rész). *ELEKTRONET*, XXIV(8):28–30, 2015.
- [N3] *L. Jani* and *Z. Á. Mann*. Megosztott cache heterogén multiprocesszoros rendszerekben (2. rész). *ELEKTRONET*, XXV(1):30–32, 2016.

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DOI:10.1109/TC.2013.127.
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