Low-power CMOS logic circuits and their design methodology

Ph.D. thesis

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1 Introduction

Power dissipation becomes a major concern in VLSI design as the feature size decreases and the corresponding chip density and operation frequency increases. The power consumption of a silicon chip and the corresponding heat dissipation determines its reliability and lifetime [Mark, 2006]. The need for low power computing forces the designers to reduce the power consumption of digital systems. The trend is driven primarily by the expensive packaging and cooling requirements [Pedram, 1996] and by the demand for portable devices, where battery life is the primary concern. Unfortunately, it extends the already complex two-dimensional optimization problem to a third dimension: designs must be optimized for power as well as performance and area [Brodersen, 1991].

There are several approaches to reduce the power dissipation, however, the highest return on investment approach is through designing for low power. Low-power design techniques have been proposed in all level of digital circuit design: from system to device. Among these techniques, there are many approaches to build low-power circuits, but unfortunately, each one has its particular drawback. In order to alleviate these drawbacks while achieving the goal of low power consumption, the possible solutions are often combined. Despite all the effort in digital circuit design to lower the power consumption of the widely used static CMOS circuits, the desired solution has not yet achieved.

To reduce the power consumption of digital CMOS circuits an order of magnitude compared to static CMOS, a fundamentally new solution is necessary. One of such solution that recently came into attention is the adiabatic charge recovery (retractile) circuits. The power efficiency of these circuits comes from two factors: one is the reduction of the ohmic loss of the resistive elements in the current path; the second is the reuse of the energy drawn from the power supply. The adiabatic principle states the followings [Koller, 1992]:

- the power consumption of a combinational logic circuit can be arbitrary low, if the circuit is operated slowly enough,
- storing data into storage element can be accomplished at arbitrary low energy loss,
- the energy loss of copying a stored data can be arbitrary low,
- however, erasing the last copy of the stored data inevitably requires a finite, not reducible amount of energy.

Unfortunately the practical adaptability of adiabatic circuit is greatly limited by the fact that these circuits achieve the high energy-efficiency for penalty in speed of operation. This means that adiabatic circuits are most suitable for applications where low-power consumption is much more important than high-performance. Such applications are the portable, battery operated devices, medical instruments, medical devices implanted inside the human body, telemetry systems, intelligent sensors and field data acquisition units, etc.

Nevertheless the performance limitation of former adiabatic circuits can be greatly alleviated by constructing more simple logic gates that are efficient even at

high operating frequencies; thereby the application of the adiabatic circuits can be extended. Moreover, there are many advantages of the adiabatic circuits over the static ones, which can be decisive of the application of adiabatic circuits in some cases.

One of these important advantages makes the use of adiabatic circuits under consideration in mixed-signal applications, where analog and digital signals are present in the same chip [32]. In mixed-signal integrated circuits the reduction of noise from the digital part to the analog signals requires careful design consideration and special design techniques. Since the adiabatic circuits use sinusoidal signals, they attractive to reduce cross talk, since they do not generate such high-frequency harmonic noises, that the square signals do, which is used by static CMOS circuits.

Another important advantage of adiabatic circuits is their inherent pipeline structure, which makes the throughput of such circuit independent of the logic depth. This advantage is particularly attractive in digital signal processing applications, where the two-level pipeline structure can easily be utilized to increase throughput without using additional pipeline registers, which are necessary in static circuits [8]. In addition to the increase in throughput, the latency of the circuit can also be kept low by using four-phase adiabatic clocking system, where – in contrary to the one- or two-phase clocking systems – four logic depths is evaluated in one clock cycle.

An additional advantage of adiabatic circuits is that there are no such design difficulties that are present for static circuits, where the elimination of these difficulties requires careful design considerations. One of such difficulty is the hazard. The hazard is not known in adiabatic circuits, since the clock-phase evaluation of each logic stage does not allow any race situation between any signals to happen. Likewise, simultaneous signal transition is not a concern, despite of all signals are actually always changing simultaneously. This is because the adiabatic circuit is powered by a resonant power supply, which draws much lower current than the current flowing into the parasitic capacitances of the adiabatic circuit. The resonant power supply only needs external energy to compensate for the loss of the system, which is generally rather low.

Moreover it worth to mention that fabrication of adiabatic circuit does not require different technology than a static CMOS, therefore the same manufacturing process can be used, even the two types of circuit can be mixed in the same chip.

2 Aims

The goal of my work is the research of low-power logic circuits, including searching for new solutions that are improved in terms of energy loss over the existing ones that are present in the literature, and – connecting to this – developing new circuit design methodologies.

Lowering the power supply is an obvious way to lower the power consumption of static CMOS circuit [Azizi, 2005], however the penalty is the diminished performance. The adiabatic charge recovery circuits offer lower power consumption while maintaining performance. However, the existing circuit types are either not suitable for CMOS implementation [Hinman, 1993], or too complex and requires too much silicon area [Younis, 1993][Lim, 1998], or requires too much phase signals to operate [Younis, 1994], or only functional at low operation frequencies [Oklobdzija, 1997], and in some cases non-adiabatic energy losses greatly diminishes its efficiency [Gabara, 1994].

Based on this, the widespread acceptance and practical use of adiabatic circuits essentially requires to simplify the adiabatic logic gates compared to the existing ones, increase the operating frequency and throughput, while also improving its energy efficiency. In order to achieve these aim, I set the following goals to work out a new type adiabatic charge recovery logic gate:

- among the parallel current paths to charge and discharge the output capacitor there shall be one current path where only one switching element is present,
- its structure shall be simple, it shall occupy modest silicon area,
- the number of clock phase signals required to operate the circuit shall be moderate, and at the same time the its throughput shall be acceptable for practical applications,
- high frequency operation shall be possible,
- adiabatic energy loss shall play prominent part in its total energy loss, its non-adiabatic loss shall be moderate or even negligible.

By exploiting the advances in technology not only the power consumption, but also the complexity of the integrated circuits are almost doubled from year to year, while the capability of the logic and register transfer level design tools are somewhat lag behind [Lehmann, 1996]. Another important problem of the integrated circuit design is the productivity of the designer and the quality of the design.

To design today's very large-scale application specific integrated circuits it is essential to use high-level synthesis tools, to raise the abstraction level of the design. The designer can work only on an abstraction level where the number of design entities is comparatively low. For example a few logic equation can be understood, but a few thousand cannot. It requires raising the abstraction level of the design, where the number of design entities is lower, e.g. a few algorithms. In the lower abstraction level

the design is manageable only if it is partitioned into smaller pieces or using such automatic synthesis tools that can handle the given complexity.

Previous works [Athas, 1997][Athas, 1996] studied the design full adiabatic systems, but no previous work was done on synthesizing adiabatic data-path from behavioral description. The pipeline structure of the adiabatic circuits is especially attractive for digital signal processing applications, where the same operations are performed on the consecutively initiated data. Scheduling, which schedule the start time of each operations into control steps is the most critical step of high-level logic synthesis. There are plenty of different scheduling algorithms in the literature, and the pipeline scheduling is also well studied [Jun, 1994][Verhaegh, 1995], however these techniques are incapable to deal with scheduling of operations performed by adiabatic functional units, since they do not take multiplexer delay into account, which are inserted into the data-path after scheduling. In order to overcome this problem, I set the following goals to work out new high-level synthesis scheduling algorithms:

- it shall take into account and exploit the two-level pipeline structure of adiabatic functional units,
- it shall take the clock-phase controlled evaluation of adiabatic logic stages into account,
- it shall make possible to synthesize adiabatic systems, using automatic design tools, starting from high-level behavioral description.

3 New scientific results

3.1 Improved adiabatic logic gate

1. Thesis group*: I worked out and applied to four-phase system a new adiabatic charge-recovery logic gate, which is more energy efficient than former adiabatic logic gates, occupies only moderate silicon area, moreover it can be operated at high operating frequencies and its energy efficiency does not deteriorate sharply with increasing operating frequency [1].*

1.1 Thesis*: I showed in four-phase system that in the period of charging the output capacitor the non-adiabatic energy loss can be eliminated by doubling the current path, and the whole energy loss of the logic gate can be greatly reduced using the same solution, as well as applying only one switching element in one of the current path [2].*

1.2 Thesis*: I showed in four-phase system that the operation of the logic gate can be fully adiabatic without using reverse logic and separation switches between the charge and discharge paths, by appropriately controlling the discharge path by an inverter placed in the next logic stage. I also showed that this solution can reduce the total energy loss despite of the energy loss of the additional inverter [1].*

***1.3 Thesis**: I worked out and applied to four-phase system an adiabatic charge recovery storage element, which dynamically stores one bit data, while the control signals and the input/output waveforms of the storage element totally matches of those of the logic gate, and the reliability of operation of the storage element is not diminished by increasing the switching time [3].*

3.2 Optimizing adiabatic circuits for minimal energy loss

***2. Thesis group**: I demonstrated that for minimal energy loss there is a well detectable optimum of the width of the transistors in the current path of the adiabatic circuits, which optimal width is the function of load capacitance and operating frequency. Moreover I demonstrated that this optimal transistor width exist only above a certain loading capacitance and operating frequency [2][4].*

***2.1 Thesis**: I demonstrated and confirmed by simulation of practical circuits that the theoretical expressions in the literature to size the transistors for minimal energy loss don't provide correct value, and the actual optimization should be done by simulation, taking the given circuit arrangement and its parasitic into account [2][4].*

***2.2 Thesis**: I showed in case of multi-phase systems that the energy consumption of the complete system composed of resonant power supply and adiabatic logic gates can be reduced by – instead of adding external capacitors to match the equivalent capacitances of the supply clock nodes – increasing the width of the transistors in the current path of the low capacitance supply clock nodes above the optimal value of the logic gate alone [1][5].*

3.3 High level synthesis of adiabatic circuits

***3. Thesis group**: I stated that the pipeline structure of adiabatic logic circuits and the clock-phase controlled evaluation of adiabatic logic stages gives adiabatic circuits an advantage in applications, where the same sequence of operations are performed on consecutively initiated data, like in digital signal processing applications. Moreover I showed that in order to automate the design of adiabatic circuits, it is necessary to extend the existing scheduling algorithms, and I worked out two new scheduling algorithms to meet this demand [6][7][8].*

***3.1 Thesis**: I worked out and applied to four-phase system a new scheduling procedure, which uses the lowest amount of functional units of each type and allows high-level synthesis of the two-level pipeline adiabatic logic by uniform distribution of the number of multiplexer inputs among the same type of functional units and by taking the delay of the multiplexer operation into account [6][8].*

***3.2 Thesis**: I worked out and applied to four-phase system a new integer linear programming scheduling procedure, which gives optimal solution and makes high-level synthesis of adiabatic logic possible by taking into account the delay of the multiplexer operations, which are inserted into the data-path after scheduling. The algorithm reserves additional control steps to multiplexer operations, depending on the number of multiplexer inputs [7][8][9].*

***3.3 Thesis**: In order to describe the pipeline operation and clock-phase controlled behavior of adiabatic logic, I worked out a VHDL modeling technique, which makes the simulation of mixed adiabatic and non-adiabatic types of circuit possible. The clock-phase controlled, but still behavioral model allows acceptable simulation time even at full system simulation, therefore it can be used to gather global performance metrics and evaluation [6][8][9].*

4 Possible applications of the new scientific results

Adiabatic circuits can be considered in applications, where there is a limited power supply available, or the cooling conditions are not satisfactory; therefore the dissipation should be minimized. Some examples are space devices, medical devices carried outside or even inside the body, and field data acquisition units, which are operated mainly from battery power and external power supply is available for data transfer or to recharge only.

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