NEW METHODS FOR THE INVESTIGATION OF MODERN ELECTRONICS PACKAGING MATERIALS USING THERMAL TRANSIENT MEASUREMENTS

Thesis for PhD Degree
Collection of Research Topics and Findings

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Research background

During my research I investigated possible thermal transient testing based methodologies capable of the accurate characterization of new nanoparticle based polymers and other high end thermal interface materials. My goal was to create methods which can measure the thermal conductivity coefficient of these substances, predict their long term behavior in an accurate and reproducible way, and allow the data to be used for physical design and simulation of power-, and other semiconductor package components.

The investigation of thermal issues in semiconductor device packaging has gained importance, partly due to ever increasing integration densities (see Moore’s law and more-than-Moore approaches such as 3D integration options) which is characteristic to high end ICs, partly due to increased device performances such as increasing wattage of IGBT-s and power LEDs. To achieve higher integration, the practice of building stacked die packages is very common nowadays in case of hand-held devices and RAM packaging. The integration of chips realized by different technologies makes also possible creating solutions such as a System-in-Package (SiP). The increasing power dissipation in each of these applications is generally paired with decreasing feature sizes, elevating the power densities even higher.

Temperature related problems are present in various cutting edge industries, such as solid-state lighting, electronics vehicle traction, power distribution systems and also in high computational power hand held appliances,
where improper thermal design may cause decay of operational parameters, reduction of lifetime or ultimately component or system failure. For the reasons above, cooling of such highly integrated devices has always been a challenge for package designers and thermal engineers. One problem is that the heat transfer from the chip to the ambient takes place through a number of thermal interface layers which reside between structural elements of the package. On the package scale the most significant heat transfer mechanism is conduction, and typically the major bottleneck regions in the heat conduction path between the semiconductor junction and the ambient are the thermal interfaces between semiconductor, metal or ceramics layers. The thermal resistance of the TIM layers, including the contact thermal resistances can add up to over 50% of the total heat conduction path. The proper and accurate thermal characterization of semiconductor devices in such complex packaging is not a straightforward task.

In the first section of my thesis I introduce a methodology for the accurate and repeatable measurement of the bulk thermal conductivity coefficient of high performance, nano-polymer based thermal interface materials. In their application environment, these materials are applied in very thin layers, usually below 100µm between the two surfaces to be contacted. In order to determine their bulk thermal conductivity coefficient, by definition you need to know their exact thickness, the temperature drop between the top and bottom surfaces of the material, the surface area and the heat flux which
generate the temperature drop. Even though it sounds simple, but in realistic conditions the measurement of all of these properties is a challenging task. In my first finding I introduce a novel methodology which is based on thermal transient tests of the material, carried out at multiple layer thickness. This methodology can be well applied for most of the commonly used material types in the industry. I also discuss the possible error sources of the measurement and also a methodology for the thermal null-point calibration of the measurement system.

Once the thermal conductivity of the thermal interface materials can be tested accurately, their pre-selection for an application becomes an easier task. For a final decision however the long-term behavior of the materials has to be tested as well. In my research I created a setup, which is very similar to the one designed to measure the bulk thermal conductivity coefficient, to test the long term behavior of the TIM by periodically turning the power of the semiconductor device used for structural tests on and off. The thermal cycles created by the continuous cycles in the powering lead to the aging of the thermal interface materials which ultimately reflects in changes in their thermal performance. In case of a properly planned test setup, the change in the thermal resistance can be tracked by changes in the calculated structure functions describing the heat conduction path.

During my research on measuring the changes of TIM materials due to aging, I also studied the property variations of TIMs due to environmental condition changes,
such as humidity. I have proven that materials of certain qualities may change their thermal properties as a function of the humidity content or due to the adsorption effect corresponding to the relative humidity changes in the environment.

Knowing the thermal properties of interface materials is a key to build proper simulation models. Still the contact thermal resistances between the TIM-s and the surfaces to be joined heavily influence the behavior of the thermal model, and unfortunately their exact thermal resistance values cannot be identified by direct measurement means. In my third research topic I worked on a methodology which allows the refinement of simulation models based on real thermal test result such, that the effect of the interfacial thermal resistances will be inherently considered, making the behavior of the thermal model perfect even in the transient domain. The benefit of such thermal models is that they exactly behave as the real device would, therefore they can be used for rapid virtual prototyping. Simulation may support the thermal transient tests themselves. As based on the principles of thermal transient testing the captured response curve is a unit step response function initiated by a step change in the electrical powering. The initial part of the measured response function is always an electrical switching signal, which carries no thermal information. Knowing the size of the heat source and the thermal properties of the die, the missing part of the thermal response can be properly simulated. As part of my third finding I will share some research results to improve
the quality of the obtained thermal transient curve using a combined measurement and simulation approach.

In my last research topic, I use the results of the first three points to accurately determine the junction-to-case thermal resistance of large area power packages with multiple heat-sources. The measurement of the $R_{thJC}$ is based on the JEDEC JESD 51-14 standard today, the so called transient dual interface method. This standard is defined for discrete packages only, and the applicability for multi heat-source devices is restricted, as the change in the boundary conditions during the two tests may significantly change the direction of the heat-flux. Nevertheless, it is frequently used in practice to characterize multi heat-source packages as well. In the description of my final research topic I highlight the potential problem with the measurement of the $R_{thJC}$ of multi heat source packages and introduce a method to overcome the problem.
New scientific results

1. Research topic: Accurate bulk thermal conductivity measurement of TIM materials using thermal transient testing

Finding 1.

I have elaborated a new methodology for the accurate and repeatable bulk thermal conductivity measurement of high performance (up to 20 W/mK) thermal interface materials. The new method combines the benefits of the currently accepted ASTM D5470-12 test standard and the benefits of thermal transient testing, without the need for using thermocouples. During the tests the thermal interface material to be measured is placed between the cooling surface of a power semiconductor package and a cooling block of similar surface shape, kept at constant temperature. By changing the distance between the two grips in fine steps and measuring the thermal impedance curve at each step, based on the obtained $R_{th}$ vs. BLT function the thermal conductivity of a material can be clearly determined.
Finding 1.1

I have elaborated a methodology to obtain the $R_0$ value, the intrinsic thermal resistance of the test setup. In the new method, I use corrosive liquid metal to ‘thermally bind’ the grips of the tester, reducing the interfacial thermal resistance between the empty grips close to 0 K/W. Based on the difference of the thermal resistance measured with the sample placed between the grips and the $R_0$ value, the effective thermal resistance (including the effect of the interface thermal resistances) can be calculated based on the following equation:

$$k_{eff} = \frac{d}{(R_{total} - R_0)A},$$

where $d$ is the distance between the grips of the tester, $R_0$ is the thermal resistance of the tester itself and $R_{total}$ is the sum of the thermal resistance of the sample, the contact thermal resistances and $R_0$.

Finding 1.2

I have elaborated a methodology for the test of the structural integrity of the test system. The methodology is based on the fact that the $R_{thJC}$ (junction-to-case thermal resistance) of the power semiconductor component used in the tester is independent from the quality of the measured TIM material. This way each and every structure function obtained by the test system should overlap until the $R_{thJC}$ value. Storing a reference structure function taken after the calibration of the test system, and comparing it with the actual measurement data allows the identification of
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changes in the calibration of the tester, or structural defects in the power semiconductor used as a heater/sensor device.
2. **Research topic: A thermal transient testing based methodology to track the material changes and reliability of thin films and TIM materials**

**Finding 2.**

I have elaborated a new methodology for testing the long term stability of highly conductive thermal interface materials.

In the methodology, the material to be tested is applied between the cooling surface of a power semiconductor device and a cold-plate. Aging of the TIM occurs by periodical powering of the semiconductor die and is tracked by thermal transient responses measured in the die area. The strength of the methodology is that the structure functions calculated based on the measured transient responses can be used to identify the physical location of the degradation in a complex, multi-layered system.

**Finding 2.1**

Using the new methodology, I have demonstrated that in case of thermal greases and pastes the thermal cycles induced by the continuous power change may increase the effective thermal conductivity of the TIM, as the cyclical temperature changes allow the material to spread between the matching surfaces better, resulting in lower thickness and/or interfacial thermal resistances.
**Finding 2.2**

I have demonstrated, that the HAST tests used widely in the industry as a standard environmental test (135°C, 2 bar, 100% RH), may fill up the TIM matrix and the voids between the TIM and the matching surfaces with humidity, temporarily increasing the effective thermal conductivity of the tested material. I have shown that the presence of the humidity and the drying process can be tested using thermal transient test method.

**Finding 2.3**

Based on the results shown in Finding 2.2 I have elaborated a new methodology to measure the humidity level of porous layers using thermal transient test methods. Following the pattern of the above introduced method, the layer to be tested is put between a heat source (power semiconductor package, resistor, etc...) and a cooled surface, assuring that the tested layer is part of the main heat-flow path. The humidity content of the layer is inverse proportional to thermal resistance, which can be accurately tested this way.

**Finding 2.4**

Using experimental methods, I have demonstrated that the measurement method proposed in Finding 2.1 is also applicable for the measurement of the relative humidity of gas mixtures, if a proper porous sensor layer is selected. I have proven experimentally that the thermal resistance of a porous silicon oxide layer located beneath a micro-meander heater changes as a function of the relative humidity of the environment.
3. Research topic: A methodology to refine the model parameters of multi-layer numerical package models based on thermal transient test data

Finding 3.

I have elaborated a methodology for the refinement of material parameters and layer thickness values for simulation studies. The methodology relies on the iterative comparison of a structure function calculated based on the transient simulation results of a detailed package model with nominal parameters, and a structure function calculated based on thermal transient measurements taken on a real physical device.

Finding 3.1

• In the new methodology the physical parameters of the layer structure of the package are aligned such, that the measurement and simulation based structure functions overlap each other.

• The structure functions are aligned to each other in an iterative way, starting from the thermal and geometrical parameters of the die, followed by the die attach layer, because the thermal capacitance and thermal resistance values obtained from the structure functions can be directly applied here. Due to the true one-dimensional nature of the heat spreading in this
early section, the information provided by the structure functions is most accurate here. Layers located farther from the heat-source, such as different ceramics, or metallic layers have usually well-known parameters, still if they don’t fit, their effective thermal conductivity coefficient should be aligned.

- The calibration process ends when the measurement and simulation based structure functions match over a thermal resistance region which corresponds to the package to be calibrated.

**Finding 3.2**

Based on the results of the research corresponding to Finding 3. I have shown that the early part of the thermal transient response which is covered by an electrical transient can be regained using thermal simulations. Using the methodology above, based on the thermal part of the measured transient response, the thermal model of the device can be calibrated. The calibrated thermal model’s simulated transient result will inherently contain the early, missing thermal transient section of the measured result. This allows the simulation based electric transient correction of the measured transient response.
4. **Research topic: RthJC measurement limits of high surface area power semiconductor devices**

**Finding 4.**

I have experimentally demonstrated that the transient dual interface methodology provides inaccurate results. The reason of the inaccuracy is the change of the heat spreading geometry in the same package at the different boundary conditions.

**Finding 4.1**

I have demonstrated with experiments and simulations that in case of those power packages, where the cooling area is significantly larger than the heated area of the semiconductor itself, the geometry of the heat-spreading changes already inside the heat spreader, when the dual interface method is applied. The change in the heat spreading geometry causes an early separation point of the structure functions. After the separation point the structure functions run parallel to each other, until the main heat trajectory reaches the real package boundary where the two curves start to diverge significantly. Identifying the first point of separation as the $R_{thJC}$ value leads to an underestimation of the thermal resistance, therefore the second separation point has to be used after the parallel section.
**Finding 4.2**

I have experimentally demonstrated that in case of multi-heat source packages the ratio of the $R_{thJC}$ value measured from one heat source and the $R_{thJC}$ value measured from $n$ heat sources powered together is not the expected $1:n$ value. The $1:n$ assumption is an underestimation of the real thermal resistance due to the overlapping of the heat-spreading cones.
Industrial application of the research results

My research topics although mostly carried out in the framework of EU supported research projects at BME, are also closely related to my work at Mentor Graphics Ltd., therefore each of my findings are somehow related to industrial needs, and some of them even inspired actual product development.

My first research topic, which covers an accurate and reproducible test method for the thermal conductivity coefficient measurement of TIM materials was used as the base idea for the DynTIM, thermal conductivity measurement instrument, which is still part of Mentor Graphics’ product portfolio. By today more than 30 companies use the system on a daily basis for their product development.

The findings of the second, third and fourth research topics serve as references for Mentor Graphics customers today, in order to allow them to do better material selection or to refine their thermal models, or to perform more sophisticated $R_{thc}$ measurements. The model refinement inspired our software team to elaborate a method capable of running several test scenarios automatically, allowing the user to find the optimal simulation parameters more easily. As of today about 80% of our customer base in Japan has adopted this method.
Publications corresponding to research topics

1. Research topic

1. Vass-Várna András, Sárkány Zoltán, Rencz Márta, 
   “Characterization method for thermal interface 
   materials imitating an in-situ environment” 

2. Andras Vass-Varnai, Sandor Laky, Zoltan Sarkany, 
   Csaba Barna, Marta Rencz: 
   “Issues of finding a proper golden-reference sample for 
   TIM tester calibration” 
   In: Proceedings of the 29th IEEE Semiconductor 
   Thermal Measurement and Management Symposium 
   (SEMI-THERM). San Jose, USA, 2013.03.17- 

3. Andras Vass-Varnai, Zoltan Sarkany, Barna Csaba, 
   Sandor Laky, Marta Rencz, 
   “A possible method to assess the accuracy of a TIM 
   tester” 
   In: International conference on Electronics 
   Packaging, ICEP 2013. Place and date of conference: 

4. Andras Vass-Varnai, Zoltan Sarkany, Gabor Farkas, 
   Marta Rencz, 
   “Industrial Need for Accurate and Reproducible 
   Measurements of Thermal Interface Materials” 
   In: International conference on Electronics 
   Packaging, ICEP-IAAC 2012. Tokyo, Japan, 17/04/2012- 

   In: Proceedings of eTherm'08 - The 1st International Symposium on Thermal Design and Thermophysical Property for Electronics. Tsukuba, Japan, 2008.06.18-2008.06.20. pp. 73-76.


   Electronics Packaging Technology Conference (EPTC), 2010 12th , vol., no., pp.279,284, 8-10 Dec. 2010, doi: 10.1109/EPTC.2010.5702648

2. Research topic

1. András Vass-Vármai, Márta Rencz,
   “Package hermeticity testing with thermal transient measurements”

2. Vass-Varnai, A.; Sarkany, Z.; Rencz, M.,
   “Reliability testing of TIM materials with thermal transient measurements”,

3. Vass-Varnai, A.; Sarkany, Z.; Rencz, M.,
   “Method for in-situ reliability testing of TIM samples”,

4. András Vass-Vármai, Péter Fürjes, Márta Rencz,
   “Possibilities of Humidity Sensing with Thermal Transient Testing on Porous Structures”,

5. A. Vass-Vármai, M. Rencz,
   “Package Hermeticity Testing with Thermal Transient Measurements”,
3. Research topic


5. Bornoff, R.; Vass-Varnai, A.,
“A detailed IC package numerical model calibration methodology”
doi: 10.1109/SEMI-THERM.2013.6526807

6. A Vass-Várnai, B Plesz, Z Sárkány, A Malek, M Rencz,
“Application of Thermal Transient Testing for Solar Cell Characterization”,

7. Ouyang, E.; Ahn, B.; Bornoff, R.; Weikun He; Islam, N.; Gwang Kim; KyungOe Kim; Vass-Varnai, A.,
“Transient thermal characterization of a fcBGA-H device”,
doi: 10.1109/SEMI-THERM.2013.6526809

8. Yake Fang, Gang Wang, Chen Xiaodan, Hon Wong Voon, Fu Xing, Andras Vass-Varnai,
“Detailed Analysis of IC Packages Using Thermal Transient Testing and CFD Modelling for Communication Device Applications”,
In: Proceedings of the 22nd International Workshop on THERMAL INvestigation of ICs and Systems (THERMINIC'16).: Budapest, Hungary
4. Research topic

1. **András Vass-Várnai**, Shan Gao, Zoltán Sárkány, Jongman Kim, Seogmoon Choi, Gábor Farkas, András Poppe, Márta Rencz,
   “Issues in junction-to-case thermal characterization of power packages with large surface area”,

Publications not directly related to this thesis

1. Attila Szel, Zoltan Sarkany, Marton Bein, Robin Bornoff, **Andras Vass-Varnai**, Marta Rencz,
   “Mission profile driven component design for adjusting product lifetime on system level”,

2. Attila Szel, Zoltan Sarkany, Marton Bein, Robin Bornoff, **Andras Vass-Varnai**, Marta Rencz,
   “Lifetime estimation of power electronics modules considering the target application”,
3. Zoltan Sarkany, **Andras Vass-Varnai**, Sandor Laky, Marta Rencz, 
   “Thermal Transient Analysis of Semiconductor Device 
   Degradation in Power Cycling Reliability Tests with 
   Variable Control Strategies”, 
   In: Proceedings of the 30th IEEE Semiconductor 
   Thermal Measurement and Management Symposium 
   (SEMI-THERM'14). 259 p. San Jose, USA, 09/03/2014- 
   4799-4374-6) 
4. Zoltan Sarkany, **Andras Vass-Varnai**, Marta Rencz, 
   “Comparison of different power cycling strategies for 
   accelerated lifetime testing of power devices”, 
   In: Electronics System-Integration Technology 
   Conference (ESTC), 2014. Helsinki, Finland, 
5. Zoltan Sarkany, **Andras Vass-Varnai**, Marta Rencz, 
   “Separation of failure modes in short cycle time power 
   cycling experiments”, 
   In: Proceedings of the 20th International 
   Workshop on THERMal INvestigation of ICs and Systems 
   (THERMINIC'14).: London, England, 24/09/2014- 
   26/09/2014., 
   Paper 1021. 5p. 
6. Zoltan Sarkany, **Andras Vass-Varnai**, Marta Rencz, 
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   IGBT structures during active power cycling tests”, 
   In: Proceedings of 16th Electronics Packaging 
   Technology Conference (EPTC'14), Singapore, 
7. Zoltan Sarkany, Andras Vass-Varnai, Gusztav Hantos, Marta Rencz,
“Failure prediction of IGBT modules based on power cycling tests”,

“Impact of nonlinearities in boundary conditions on device compact thermal models”,

9. Zoltan Sarkany, Andras Vass-Varnai, Marta Rencz,
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10. Andras Vass-Varnai, John Parry, Gergely Toth, Sandor Ress, Gabor Farkas, Andras Poppe, Marta Rencz,
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11. B Plesz, Gy Horváth, **A Vass-Vármai**, “Characterization of solar cells by thermal transient testing”,


13. András Poppe, **Andras Vass-Varnai**, Gábor Farkas, Marta Rencz
   “Package characterization: simulations or measurements?”,
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14. L Juhász, A Vass-Vármai, C Dominkovics, V Timár-Horváth:
   “Porous Al2O3 Layers for Capacitive RH Sensors”,

16. **Veronika Timár-Horváth**, László Juhász, **András Vass-Várna**, Gergely Perlaky,

17. Veronika Timár-Horváth, László Juhász, **András Vass-Várna**, Gergely Perlaky,
   “Usage of Porous Al2O3 Layers for RH Sensing”,