NEW METHODS FOR THE INVESTIGATION OF MODERN ELECTRONICS PACKAGING MATERIALS USING THERMAL TRANSIENT MEASUREMENTS

Thesis for PhD Degree

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Nyilatkozat önálló munkáról, hivatkozások átvételéről

Alulírott Vass-Vármai András kijelentem, hogy ezt a doktori értekezést magam készítettem és abban csak a megadott forrásokat használtam fel. Minden olyan részt, amelyet szó szerint, vagy azonos tartalomban, de átfogalmazva más forrásból átvettem, egyértelműen a forrás megadásával megjelöltem.

Nyilatkozat nyilvánosságra hozatalról

Alulírott Vass-Várnai András hozzájárulok a doktori értekezésem Interneten történő nyilvánosságra hozatalához, korlátozás nélkül.

Abstract

During my research, I investigated possible thermal transient testing based methodologies capable of the accurate characterization of new nanoparticle based polymers and other high end thermal interface materials. My goal was to create methods which can measure the thermal conductivity coefficient of these substances, predict their long-term behavior in an accurate and reproducible way, and allow the data to be used for physical design and simulation of power-, and other semiconductor package components.

The investigation of thermal issues in semiconductor device packaging has gained importance, partly due to ever increasing integration densities (see Moore’s law and more-than-Moore approaches such as 3D integration options) which is characteristic to high end ICs, partly due to increased device performances such as increasing power consumption of IGBT-s and power LEDs. To achieve higher integration, the practice of building stacked die packages is very common nowadays in case of hand-held devices and RAM packaging. The integration of chips realized by different technologies makes also possible creating solutions such as a System-in-Package (SiP). The increasing power dissipation in each of these applications is generally paired with decreasing feature sizes, elevating the power densities even higher.

Temperature related problems are present in various cutting edge industries, such as solid-state lighting, electronics vehicle traction, power distribution systems and also in high computational power hand held appliances, where improper thermal design may cause decay of operational parameters, reduction of lifetime or ultimately component or system failure.

For the reasons above, cooling of such highly integrated devices has always been a challenge for package designers and thermal engineers. One problem is that the heat transfer from the chip to the ambient takes place through several thermal interface layers which reside between structural elements of the package. On the package scale the most significant heat transfer mechanism is conduction, and typically the major bottleneck regions in the heat conduction path between the semiconductor junction and the ambient are the thermal interfaces between semiconductor, metal or ceramics layers. The thermal resistance of the TIM layers, including the contact thermal resistances can add up to over 50% of the total heat conduction path. The proper and accurate thermal characterization of semiconductor devices in such complex packaging is not a straightforward task.

In the first section of my thesis I introduce a methodology for the accurate and repeatable measurement of the bulk thermal conductivity coefficient of high performance, nano-polymer based thermal interface materials. In their application environment, these materials are applied in very thin layers, usually bellow 100µm between the two surfaces to be contacted. In order to determine their bulk thermal conductivity coefficient, by definition you need to know their exact thickness, the temperature drop between the top and bottom surfaces of the material, the surface area and the heat flux which generate the temperature drop. Even though it sounds simple, but in realistic conditions the measurement of these properties is a challenging task. In my first finding I introduce a novel methodology which is based on thermal transient tests of the material, carried out at multiple layer thickness. This methodology can be well applied for most of the commonly used
material types in the industry. I also discuss the possible error sources of the measurement and a methodology for the thermal null-point calibration of the measurement system.

Once the thermal conductivity of the thermal interface materials can be tested accurately, their pre-selection for an application becomes an easier task. For a final decision, however the long-term behavior of the materials has to be tested as well. In my research, I created a setup, which is very similar to the one designed to measure the bulk thermal conductivity coefficient, to test the long term behavior of the TIM by periodically turning the power of the semiconductor device used for structural tests on and off. The thermal cycles created by the continuous cycles in the powering lead to the aging of the thermal interface materials which ultimately reflects in changes in their thermal performance. In case of a properly planned test setup, the change in the thermal resistance can be tracked by changes in the calculated structure functions describing the heat conduction path. During my research on measuring the changes of TIM materials due to aging, I also studied the property variations of TIM-s due to environmental condition changes, such as humidity. I have proven that materials of certain qualities may change their thermal properties as a function of the humidity content or due to the adsorption effect corresponding to the relative humidity changes in the environment.

Knowing the thermal properties of interface materials is a key to build proper simulation models. Still the contact thermal resistances between the TIM-s and the surfaces to be joined heavily influence the behavior of the thermal model, and unfortunately their exact thermal resistance values cannot be identified by direct measurement means. In my third research topic I worked on a methodology which allows the refinement of simulation models based on real thermal test result such, that the effect of the interfacial thermal resistances will be inherently considered, making the behavior of the thermal model perfect even in the transient domain. The benefit of such thermal models is that they exactly behave as the real device would, therefore they can be used for rapid virtual prototyping.

Simulation may support the thermal transient tests themselves. As based on the principles of thermal transient testing the captured response curve is a unit step response function initiated by a step change in the electrical powering. The initial part of the measured response function is always an electrical switching signal, which carries no thermal information. Knowing the size of the heat source and the thermal properties of the die, the missing part of the thermal response can be properly simulated. As part of my third finding I will share some research results to improve the quality of the obtained thermal transient curve using a combined measurement and simulation approach.

In my last research topic, I use the results of the first three points to accurately determine the junction-to-case thermal resistance of large area power packages with multiple heat-sources. The measurement of the $R_{thJC}$ is based on the JEDEC JESD 51-14 standard today, the so called transient dual interface method. This standard is defined for discrete packages only, and the applicability for multi heat-source devices is restricted, as the change in the boundary conditions during the two tests may significantly change the direction of the heat-flux. Nevertheless, it is frequently used in practice to characterize multi heat-source packages as well. In the description of my final research topic I highlight the potential problem with the measurement of the $R_{thJC}$ of multi heat source packages and introduce a method to overcome the problem.
Acknowledgements

First and foremost, I would like to thank my advisor, Professor Marta Rencz. Marta encouraged me to begin my PhD studies, and she guided me all the way. She taught me how to approach a research topic, plan experiments and share my findings in form of publications. I appreciate all her contributions of time, ideas, professional and sometimes personal toned conversations and many forms of support, which made me confident and led me to create this thesis. I am also thankful for the excellent example she has provided as a successful scientist and always kind and caring advisor.

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# Nomenclature

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<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
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<tbody>
<tr>
<td>A</td>
<td>Area (cm²)</td>
</tr>
<tr>
<td>c</td>
<td>Specific heat capacity (J/kgK)</td>
</tr>
<tr>
<td>c_v</td>
<td>Volumetric heat capacity (J/m³K)</td>
</tr>
<tr>
<td>C_th</td>
<td>Thermal capacitance (J/K)</td>
</tr>
<tr>
<td>Q</td>
<td>Heat flux (W/cm²)</td>
</tr>
<tr>
<td>R_th</td>
<td>Thermal resistance (K/W)</td>
</tr>
<tr>
<td>R_thJA</td>
<td>Thermal resistance from junction-to-ambient (K/W)</td>
</tr>
<tr>
<td>R_thJC</td>
<td>Thermal resistance from junction-to-case (K/W)</td>
</tr>
<tr>
<td>T</td>
<td>Temperature (K)</td>
</tr>
<tr>
<td>t</td>
<td>Thickness (cm)</td>
</tr>
<tr>
<td>τ</td>
<td>Thermal time constant (sec)</td>
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<tr>
<td>λ</td>
<td>Bulk thermal conductivity (W/mK)</td>
</tr>
<tr>
<td>ρ</td>
<td>Density (kg/m³)</td>
</tr>
<tr>
<td>θ</td>
<td>Thermal resistance per unit area (Kcm²/W)</td>
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<tr>
<td>BLT</td>
<td>Bond Line Thickness</td>
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<tr>
<td>CFD</td>
<td>Computational Fluid Dynamics</td>
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<tr>
<td>CNT</td>
<td>Carbon Nanotube</td>
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<tr>
<td>CSF</td>
<td>Cumulative Structure Function</td>
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<tr>
<td>DUT</td>
<td>Device Under Test</td>
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<tr>
<td>DSF</td>
<td>Differential Structure Function</td>
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<tr>
<td>EDA</td>
<td>Electronics Design Automation</td>
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<tr>
<td>FEM</td>
<td>Finite Element Methodology</td>
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<tr>
<td>HAST</td>
<td>Highly Accelerated Stress Test</td>
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<tr>
<td>IGBT</td>
<td>Insulated Gate Bipolar Transistor</td>
</tr>
<tr>
<td>LED</td>
<td>Light Emitting Diode</td>
</tr>
<tr>
<td>MCAD</td>
<td>Mechanical Computer Aided Design</td>
</tr>
<tr>
<td>MCPCB</td>
<td>Metal Core Printed Circuit Board</td>
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<tr>
<td>MQFP</td>
<td>Metric Quad Flat Pack</td>
</tr>
<tr>
<td>NID</td>
<td>Network Identification via Deconvolution</td>
</tr>
<tr>
<td>RH</td>
<td>Relative Humidity</td>
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<tr>
<td>SiP</td>
<td>System in Package</td>
</tr>
<tr>
<td>SWCNT</td>
<td>Single Wall Carbon Nanotube</td>
</tr>
<tr>
<td>TIM</td>
<td>Thermal Interface Material</td>
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1. Research topic: Measurement of the bulk thermal conductivity of Thermal Interface Materials using thermal transient testing

Overview of TIM development trends and test methods

In the first chapter I present some recent trends in thermal interface material (TIM) development, and outline the state of the art in testing interface thermal resistance values. The available experimental techniques are presented shortly, and the currently available industrial methods are discussed in more details. In the overview special emphasis is put on presenting the Structure Function method that is applicable to measure partial thermal resistances “in situ” that is to measure the thermal resistance of the thermal interface material used as the die attach in packages.

Characterization of thermal properties of Thermal Interface Materials (TIMs) has gained increasing importance as the relative percentage of overall semiconductor package material thermal resistance attributed to the TIMs has increased. The development of new TIMs has resulted in materials with very high performance and in certain instances with very thin in-situ application thickness, giving very small thermal resistance values. As the high power densities request for even better performing thermal interface materials we will soon face the challenge of measuring $R_{th}$ values that the current technology is not able to test, or at least not with such a high throughput that would allow to apply the methodology in manufacturing testing.

These trends have placed increasing focus on the methods to characterize the thermal conductivity of TIM materials and in-situ $R_{th}$ values, to the development of characterization equipment, and to verify the accuracy and repeatability of results. My first research topic intends to answer some of these challenges in the industry.

Thermal interface material is used at several layers in complex packages - stacked die packages contain as many TIM layers as the number of stacks - but we usually distinguish TIM1 and TIM2 layers even at single die processor packages, see Figure 1-1 [1].

TIM1 is the biggest challenge to test, as it is in contact with the chip itself and it is normally difficult to access. On the other hand, the quality of TIM1 is usually responsible for the reliability of the package and the whole operation of the chip, since any void or manufacturing problem in the TIM1 layer may result in overheating and destroying the chip during the operation. Note that although several very important other mechanical properties have to be achieved to have a good TIM material, in this research topic I focus the discussion primarily to the consideration and characterization of the bulk thermal conductivity, as the most important parameter from the thermal management’s point of view.
New methods for the investigation of modern packaging materials using thermal transient testing

Figure 1-1: Typical IC package structures, showing TIM1 and TIM2 placement for bare die package and lidded package [1]

Trends in TIM development

Common TIMs include a variety of polymer-based materials with high thermal conductivity particle inclusions, typically with diameters of 2-25 μm. The effective thermal conductivities of particle-filled polymer interface materials are typically about an order of magnitude higher than the polymer matrix alone, i.e. of the order of 2-4 W/mK.

The operation principle of TIMs is relatively simple, with the pressure applied on the sample the particles within the matrix congest and create thermal ‘corridors’ between the two contacting surfaces. However, the resistance found in commercial products can be substantially larger than the anticipated values (typically 0.1 Kcm²/W) owing to resistances at the TIM boundaries and small voids. This has motivated the recent progress on using solders, which may provide conductivities in the range of 10-100 W/mK, but due to their mechanical stiffness these metallic TIMs are less attractive for TIM1 application. The application thickness of TIM materials is small compared to other package features. In case of greases it spans between a few tens to a few hundreds of microns, while commonly used elastic pads are thicker, they can reach up to a few millimeters in thickness.

Figure 1-2: Resistance model of a typical thermal interface

The thermal resistance of the interface layer consists of three different thermal resistance values, the thermal resistance of the material itself and the interface thermal resistances between the TIM material and the surfaces to be connected, as shown in Figure 1-2. The research for better
performing TIM materials is aimed at the reduction of the total thermal resistance of the interface, following three different approaches:

- Increase of the bulk thermal conductivity by using highly conductive fillers
- Decrease of the bondline thickness of the interface
- Decrease of the interfacial thermal resistances

Figure 1-3 introduces a few experimental solutions to address the points summarized above [2]. Figure 1-3 (a) demonstrates a vertically aligned carbon nanotube (CNT) interface. CNTs were expected to solve all the problems of high conductivity TIM material as their theoretical thermal conductivity was reported extremely high, but the values that could have been measured in manufactured TIM material so far have disappointed the engineering community. CNTs possess in fact an exceptionally high thermal conductivity in the axis direction according to molecular dynamics simulations and experimental measurements. For an individual single wall carbon nanotube (SWCNT), it can be as high as 5000-8000 W/mK [3],[4],[5],[6] and that of an individual multi wall carbon nanotube can reach 3000 W/mK [7]. Thus CNTs have a great potential to be employed for integrated circuit thermal management applications. Growing CNTs between interfaces is not an obvious task at all, therefore there are other attempts as well to apply them as TIMs. As high thermal conductivity of the filler is needed in TIM materials for high performances CNTs with their outstanding thermal conductivity are obvious candidates. It is reported that the use of dispersed CNTs as thermal conducting fillers in polymer composites has resulted in an increase above 50% of the thermal conductivity [8],[9] achieving a measured thermal conductivity of 40 W/mK. But the enhanced values are still not satisfactory due to several problems:

- The existence of interface thermal resistances, see Figure 1-2,
- Non perfect crystalline structure of the CNTs,
- Non uniform dispersion of CNTs in epoxy resins,
- Weak bond between CNT and the epoxy material, resulting in increased interfacial resistance.
Figure 1-3 (b) describes an experimental material where two different fillers were applied to the matrix. Beside the larger, micrometer sized fillers (indicated in white in the image), smaller, nanometer sized fillers are also used (indicated with blue color). The smaller fillers are used to increase the area of the heat transfer and also to decrease the contact resistances.

Figure 1-3 (c) shows an experimental solution do decrease the contact thermal resistances. In this method the surfaces to be connected are covered with a special material, called nano-sponge [10], which is capable of adjusting itself to the fillers in the matrix, resulting in a higher contact area.

As a conclusion, the use of nanoparticles and nanotubes is almost inevitable in finding better performing TIM material. The research and development in this field has to focus on minimizing the total thermal resistance rather than just increasing the thermal conductivity. Minimizing the contact resistance and the bond line thickness will become a more and more important issue in realizing thin highly conducting TIMs.

**Techniques used today to characterize TIM performance [11]**

The major challenge in TIM testing is caused by the fact that there is a significant difference between standardized lab test data and application-specific (or “in-situ”) test results in a specific set of application conditions. Standardized test methodologies are mandatory because the industry has the right to a fair comparison between various TIMs from various vendors [12, 13].

Measuring the thermal conductivity is not easy in general. The $\lambda$ (or sometimes $k$) thermal conductivity is the intrinsic property of a material that indicates its ability to conduct heat. It is defined as the quantity of heat, $Q$, transmitted in time $t$ through a thickness $L$, in a direction normal to a surface of area $A$, due to a temperature difference $\Delta T$, under steady state conditions and when the heat transfer is dependent only on the temperature gradient:

$$\lambda = \frac{Q}{t} \cdot \frac{L}{A \cdot \Delta T} \quad (1-1)$$

To measure it you should know the exact values of the quantities in equation (1-1), which is normally very hard to achieve in case of realistic TIMs. E.g. looking at Figure 1-2 it is easy to understand that the layer thickness is not uniform, consequently the temperature values along the interface will be also different, and assuring uniform heat flux along the sample is also extremely difficult. This explains why is TIM testing in the focus of academic and industrial research today, when the high quality TIM manufacturing needs appropriate measurement methods.

The extremely increased TIM material performance is very difficult to follow by the currently available measurement techniques. The requirements here are twofold. First techniques are needed to characterize the TIM material in itself, independently from the future applications. For this purpose, complex, very expensive and slow techniques are also acceptable, as these measurements do not have to be done in very high volumes. I call them now experimental methods. To characterize the TIM performance in a given electronics application, e.g. to find the $R_{th}$ value of a TIM1 layer in a processor package during manufacturing testing raises new requirements: these measurements
have to be very fast in situ measurements with somewhat less demanding accuracy requirements. I call them here now industrial methods.

**Experimental methods**

Some of the major experimental methods used today to characterize TIM performance are briefly presented below.

Direct measurement of the thermal properties on special samples

Figure 1-4 presents a potential arrangement for measuring the thermal diffusivity (that is the ratio of the thermal conductivity to the volumetric heat capacity) of a dedicated sample if thermal sensors are manufactured at the interfaces.

A driving force (temperature difference, electronic potential, energetic laser pulse, etc. depending on the method) induces interactions on atomic or molecular level. This response allows to obtain insight into the physical properties of the thermal interface, allowing to measure the thermal resistance, the thermal conductivity/diffusivity, the interface resistance and the electrical conductivity on a continuum or sub-micron scale. The measurement techniques can be either static or transient, each of which has certain advantages with respect to sensitivity to a specific physical property (e.g. diffusivity or conductivity), resolution or applicability. The method needs special sample preparation, and maintaining uniform thickness is not easy. The cost and the accuracy of the experimental measurement are determined by the accuracy of the apparatus used for heating and measuring.
Transient thermo-reflectance measurement

The transient thermo-reflectance method (TTR) [14] is a frequently used experimental technique to determine the thermal conductivity of thin film and multilayered materials. It is a non-contact and non-destructive optical approach, both for heating a sample under test and for probing the variations of its surface temperature [15]. As the method is non-invasive, it is attractive for the measurement of the thermal properties of thin-layer materials as well.

The basic principle of the transient thermal reflectance method is to heat a sample by laser irradiation and probe the changes in the surface reflectivity of the heated material. The source of energy in the TTR method is normally provided by a pulsed laser with short pulse duration.

During each pulse, a given volume on the sample surface heats up to a temperature level above ambient due to the laser light energy absorbed by the sample. The heating area is specified by adjusting the pulsing laser aperture and the optics of the system. The depth of the volumetric heating, on the other hand, is determined by the optical penetration depth, which is a function of laser wavelength and surface material properties. After each laser pulse is completed, the sample begins to cool down to the initial ambient temperature. During this process, the probing laser light reflected from the sample surface at the heating spot center is collected on a photo detector that reads the instantaneous surface reflectivity. The influence of a pulsed laser irradiation on a given material depends both on the optical properties of that material as well as on the wavelength and pulse duration of the laser itself. This makes the technique rather complex and its everyday application for TIM testing at this moment seems rather improbable.
The 3 omega method

The 3-omega technique was developed by Cahill [17]. It is similar to the hot-wire technique in that it utilizes radial flow of heat from a single element which is used both as a heater and a thermometer. The major difference is the use of the frequency dependence of a temperature oscillation instead of a time domain response.

![Figure 1-6: The 3 Omega Method [17]](image_url)

A narrow heating element is deposited on the sample to form a narrow line source of heat on the surface of an infinite half volume using either photolithography or evaporation through a mask.

An AC power of controllable frequency is supplied to the heater, and the temperature response of the heater is determined from its thermal impedance. The thermal conductivity is determined from the power and the third harmonics of the voltage oscillations. Recent papers question however the accuracy of the method [18], demonstrating that complex error correction is needed to obtain accurate thermal conductivity results with the method.

The above listed techniques are more or less applicable for the laboratory testing of thermal conductivity values of material layers, however all of them are rather complex, need lengthy sample preparations and provide only bulk data. Carrying out such measurements takes prohibitively long time, for this reason they are not applicable for in-situ industrial applications.

**Industrial methods**

The industrial methods are either standardized methods, to allow better comparison of the measured results, or they are application specific (sometimes ad hoc) methods assuring very fast measurement to allow in-line application for reliability assessment.

The current primary steady state method: the ASTM D5470-12[19]

The ASTM D-5470 test method is a standard method to measure thermal resistance and bulk conductivity for TIMs such as pads, tapes, greases and phase change materials. The sample is placed between a hot meter bar and a cold meter bar and a steady state of heat flux is established.
The ASTM test defines thermal resistance per unit area, \( \theta \), to include the thermal resistance of the material (\( \theta_{\text{material}} \)) plus the interfacial contact resistance of the TIM to the substrates (\( \theta_{\text{interface}} \)):

\[
\theta_{\text{total}} = \theta_{\text{material}} + \theta_{\text{interface}} \quad (1-2)
\]

Fourier’s Law describing one-dimensional heat flow defines the thermal resistance per unit area of a material as:

\[
\theta_{\text{material}} = \frac{\Delta T \cdot A}{Q} = \frac{t}{\lambda_{\text{bulk}}} \quad (1-3)
\]

where \( \Delta T \) is the temperature difference across the TIM under test, \( A \) is the area of the meter bars, \( t \) is the thickness of the sample, and \( \lambda_{\text{bulk}} \) or \( k_{\text{bulk}} \) is the material bulk conductivity. The heat flux \( Q \) is either measured from the temperature drop along the meter bars length (requiring multiple temperature sensors in each bar) or it is identified by carefully determining the power supplied to the hot bar and by using guarding and/or insulation of the bars to eliminate any heat loss. Combining equations 1-2 and 1-3,

\[
\theta_{\text{total}} = \frac{\theta_{\text{interface}} + t}{\lambda_{\text{bulk}}} \quad (1-4)
\]

The ASTM method measures \( \theta_{\text{total}} \) as a function of thickness of the TIM. This plot is linear, the slope of the line is proportional to \( 1/\lambda_{\text{bulk}} \), and the intercept is a measure of \( \theta_{\text{interface}} \) (see Figure 1-8). [19].
As $\theta_{\text{interface}}$ is known to be sensitive to the testing surfaces (material type, flatness, roughness, and conditioning by previous samples), the correlation of $\theta_{\text{total}}$ to thermal test vehicles has shown correct rank order but the ASTM test under-predicted the in-situ thermal resistance [20,21,22]. This difference in absolute value was attributed to the assemblies having different surface properties compared with the ASTM tester. One advantage of the ASTM test is that equation 1-3 allows one to obtain $\lambda_{\text{bulk}}$ independent of these interfacial effects, yielding a material property. The $\lambda_{\text{bulk}}$ along with $\theta_{\text{total}}$ measured at representative pressures and gaps can be useful in selecting candidate materials for in-situ evaluation. Depending upon the TIM under consideration, the gap in-situ, and the nature of the in-situ surfaces, the contact resistance, $\theta_{\text{interface}}$, may be a large portion of the total resistance to the $\theta_{\text{total}}$ heat flow. Furthermore, it should be realized that the ASTM D5470 is only valid under the following assumptions:

- Truly one-dimensional heat flow,
- Constant thickness during measurement,
- Thickness independent contact resistance.

The one-dimensional heat flow assumption has been investigated by modeling with the conclusion that the 1D heat flow can be ensured if the meter bars are long enough, the temperature sensing holes are far enough apart and the position of these holes is known with high accuracy. The latest version of the ASTM test addresses methods to hold constant or measure the gap during the test. If the contact resistance is a function of thickness a straight line is not obtained when plotting the data according to equation 1-3, so this assumption can be tested.

Still the use of thermocouples reduces the accuracy of the ASTM method as well. Bad contacts within the meter bar may result in inaccurate temperature readings, location error of the holes in the meter bar may result in inaccurate heat flux calculations. Even longer and thinner meter bars may be a solution to decrease these inaccuracies, however such approach would result in increasing power leakage on the surface of the meter bars, which again negatively affects the accuracy of the identified heat flux.
Another important shortcoming of the ASTM method has been its use of high pressure during the test [11]. This pressure is useful in coalescing elastomeric TIM material layers which are stacked to obtain the thickness variation required for analysis using equation 1-3. In addition, the high pressure reduces the contact resistance between solid samples and the meter bars. With grease and phase change TIMs high pressure testing results in a lower gap setting than seen in most applications and if the $\theta_{total}$ is only reported at this thinnest gap, the value of $\theta_{total}$ will be lower than seen in an actual application. Most TIM vendors address this issue by publishing $\theta_{total}$ as a function of pressure so users can estimate the $\theta_{total}$ for their application. The final revision of the ASTM method has officially made provisions for lower pressure testing [19].

As a result of the error factors summarized above, even today no commercial source is available guaranteeing consistent quality. Each machine has been built uniquely for the specific user. Such a wide variety of instrumentation has led to quite significant inter-laboratory error levels.

A final drawback of this method is that the problems associated with thermal conductivity measurements are often underestimated, even by experts, because the principle seems so easy. It is recommended that users become familiar with some recent papers, e.g. [1,23,24] which discuss the issue and cover the technical difficulties of building reliable ASTM D5470-based equipment.

**Transient methods**

It is commonly believed that as transient methods are faster in general than steady state methods they are better applicable for industrial measurements. The structure function based methods allow determining partial thermal resistances in a heat flow path [25,28], based on rigorous mathematical transformation of the measured heating or cooling curves [26,27,28].

Structure functions are calculated based on the unit step response function induced by a sudden step change in the device’s input power. The resulting thermal signal is measured at the location of the powering, usually the active area, or ‘junction’ area of a semiconductor component, using electrical means. The so-obtained junction temperature change function ($T_j(t)$) is a monotonically increasing or decreasing function, depending on the heating or cooling nature of the power step. In generic applications, the temperature response is often normalized by the applied power, creating the so called $Z_{in}$, or thermal impedance curve. If all the electric energy is converted into heating power (single energy transport), the calculation of the $Z_{in}(t)$ function is very simple [29,30]:

$$Z_{in}(t) = \Delta T_j(t) / \Delta P_{el}, \quad (1-5)$$

where $\Delta P_{el}$ is the input power step. This function can be applied to give a good approximation of the junction temperature for any power step, simply by multiplying each time point by the actual heating power. Linearity is always assumed; nonlinear effects may introduce a small error for this methodology.

The thermal impedance curves usually show a ‘bumpy’ nature, as they describe the heating and cooling properties of the different mechanical components of the semiconductor, starting from...
the chip, the die attach, the package base, and finally the ambient. As the characteristic heating/cooling times can be very different for these different features, normally the thermal impedance curves are shown over a logarithmic time axis:

\[ Z_{th}(t) = R_{th} \cdot (1 - e^{-t/\tau}) \]

\[ \tau = R_{th} \cdot C_{th} \]

**Figure 1-9: Typical Zth curve corresponding to a power transistor package**

These curves can always be considered as sum of exponential functions, each corresponding to thermally significant elements in the heat conduction path, see Figure 1-9.

For a simple, uniform block of material, the thermal model consists of a simple thermal resistance expressing the conductive and a parallel connected thermal capacitance, representing the energy storing element.

**Figure 1-10: Dynamic thermal model corresponding to one single uniform material block, represented by thermal network elements (left) and by discrete time constant (right) [29]**

The unit step response function of such pair can be expressed by a closed, exponential formula. The formula contains two variables, the \( R_{th} \) (thermal resistance) and the \( \tau \) (thermal time constant) corresponding to the material block. As \( \tau = R_{th} \cdot C_{th} \) both the thermal network and the thermal time constant spectrum representation shown in Figure 1-10 describe the thermal behavior of the material block equally. In case of realistic systems however the heat penetrates through a number of such material blocks, therefore the corresponding model elements have to be connected in series. In the time constant spectrum representation several peaks appear corresponding to the time constant and thermal resistance of the blocks composing the thermal system, as shown in Figure 1-11.
The unit step response of such model will be the sum of the individual exponential functions describing the different material layers in the package:

\[ T(t) = \sum_{i=1}^{n} P_i \cdot R_{th,i} \cdot (1 - e^{-t/\tau_i}) \]  

(1-6)

The model shown in Figure 1-11 is called the Foster model of thermal impedance, and it fully describes the behavior of the thermal system and perfectly gives back the thermal impedance curve corresponding to a component for a unit step input. Matching the individual R-C pairs in the Foster model to the individual physical layers is not possible, as based on the serial connected nature, swapping any of the parallel connected R-C stages with each other would still give the same thermal response function.

Reorganizing the model to a ladder-type form, called the Cauer model however requires a fixed location of each of the thermal network elements, and properly transformed from the Foster model it can be used not only as a behavior model, but it allows the circuit elements to be directly associated with the physical layers of the analyzed thermal system.

The structure functions are practically a visual representation of the Cauer model. Commercially available methodologies generate app. 150 – 250 individual network elements, and in order to more easily interpret them, plotting the sum of the thermal capacitance values in the model over the sum of the thermal resistances will give a function which is directly characteristic to the thermal behavior of the different physical layers.
In the cumulative structure function (CSF) the origin represents the heat source. As the heat penetrates farther and farther from the origin, the isotherms embrace larger and larger volumes of material. The thermal resistance between two points of the structure function can be regarded as the thermal resistance between these isotherms, and the thermal capacitance is characteristic to the volume between the isotherms.

Flat sections will normally represent thermal interface material regions, where the thermal resistance is significant, however as TIM-s are normally applied in thin layers, the corresponding thermal capacitance is low. Steeper sections will show semiconductor or metal layers, where the thermal resistance of the material is lower, but the corresponding volume is higher.

In some cases, the material boundaries are hard to see in the cumulative form of the structure function. In such situations the derivative of the cumulative structure function may allow the identification of the interfaces better:

\[
DSF = \frac{dC}{dR} = c_v \cdot dx \cdot A \cdot \left( \frac{1}{\lambda} \cdot \frac{dx}{A} \right)^{-1} = c_v \cdot \lambda \cdot A^2
\]  

This form is called the differential structure functions (DSF), where highly conductive areas (high slope in the integral form) appear as peaks and low conductive areas (flat sections in the integral form) appear as valleys. The differential structure functions also carry information on the area of the heat conduction path.

In the following section of this chapter I describe some experiments to demonstrate how these functions are used in common practice, then I will show some novel material characterization methodologies, applying the same structural modeling technology as their basis.
New methods for the investigation of modern packaging materials using thermal transient testing

Structure function based TIM testing methods

In the example given below the measured sample contained stacked thermal test dies for verification purposes. The cross section of the measured packages is shown Figure 1-14 and the measurement arrangement is demonstrated in Figure 1-15. Each die in the package contained a resistive heater element and a diode type temperature sensor. The dies were encapsulated in a MQFP type package, which is a rectangle shaped plastic package with bent leads on each side.

![Cross section of the measured packages from the paper of [31]](image)

**Figure 1-14: Cross section of the measured packages from the paper of [31]**

![Measurement arrangement corresponding to the same project](image)

**Figure 1-15: Measurement arrangement corresponding to the same project**

In the experiment presented in details in [31] the top die was used as heater and temperature sensor. The measured package was mounted on a test board and thermal transient tests were carried out in a still air chamber environment as it is shown in Figure 1-15, then the test was repeated such that the bottom was connected to a cold plate to assure one-dimensional heat flow from the top die towards the cold plate. The thermal transient measurements on the top die were done by the T3Ster thermal transient tester and software [32].

The structure function (in blue color) shown in Figure 1-16 was constructed automatically by the measuring equipment from the measured driving point thermal impedance, referring to the top die. In this figure the horizontal axis shows the thermal resistance values measured from the heated top die towards the ambient. On the vertical axis the thermal capacitance values are shown in logarithmic scale. The first vertical step of the cumulative structure function refers to the thermal capacitance of the first element in the heat flow path that is the top die itself. The next element of the structure is the die attach under the top die: appearing with its high thermal resistance value in the figure and an almost horizontal section in the structure function. The next very steep section of the curve refers to the bottom die: both the thermal resistance of the next die attach and the thermal capacitance the second die can be read from the function. In a similar way thermal resistance/thermal capacitance values corresponding to further structural elements in the heat-flow.
path can be identified. At the end of the curve the capacitance of the lead frame and the thermal resistance from the lead frame to the cold plate can be read. These sections are indicated by a red color curve, which represents the thermal resistance and thermal capacitance of each internal layer. These ‘steps’ can be also regarded as a thermal R-C network representation, or so called ‘compact thermal model’ of the structure. As presented in the example the thermal resistance of the different TIM layers can be easily and readily read from the structure functions with very short transient measurements [28].

Another structure function based method is presented in [33] and discussed also in [11]. The simple test jig consists of a heater transistor and a rotationally symmetric metal sample holder with subsequent wider and narrower area components. The change of the geometry of the sample holder creates well identifiable peaks in the corresponding differential structure function (that is the derivative of the cumulative structure function, giving peaks at highly conductive metallic layers). The most characteristic layers of the fixture are indicated by A, B and C in Figure 1-17.

The differential structure function of the sample in Figure 1-18 shows well identifiable peaks corresponding to the A and B structures.
New methods for the investigation of modern packaging materials using thermal transient testing

**Figure 1-18.** The differential structure function of the heat flow path of the structure of Figure 1-17. A, B, and C refer to the appropriate regions, T refers to the heating transistor.

The peak at B shifts to the left if sample material is placed between the faces of the fixture. The shift in the location of the peak B gives the $R_{th}$ value of the sample. The advantage of the method is its simplicity, but to increase accuracy high precision fixture with pressure control would be required.

**Special thermal test dies**

For the sake of completeness, I have to mention also the specific thermal test vehicles that are more and more frequently used in the industrial development process to verify the measurable characteristics of the packaged circuit [34,35]. The thermal test die used in the package of Figure 1-19 is a good example for using a specific thermal test vehicle.

**Figure 1-19.** Possible measurement setup using TTV-s and the temperature-sensing matrix

This is a die with uniformly placed heater and sensors, enabling to emulate the operation of the final device in the package in order to assure optimization of the TIM technology, and other elements of the packaging for minimal junction temperature. Of course both static and transient measurements can be used to characterize the behavior of the TIM layer placed between two such thermal test dies.
A new ASTM D5470 based methodology using thermal transient testing principles

Research background

Considering the variety of available test methods introduced above, the selection of an appropriate test method for the measurement of newly developed materials is a very hard task. The members of the European Nanopack consortium faced the same concern between 2007 to 2011 [36]. Nanopack was an EU founded FP7 project with selected European companies, universities and research institutes with much experience in the field of TIM testing, led by Thales Research. One of the goals of the project was the development of new TIM material solutions while other partners worked on the realization of enhanced, in some instances highly scientific ASTM type testers which are capable of measuring TIM-s at 20 W/mK and beyond. One of the most difficult challenges in the project was the selection of proper reference materials for round robin test purposes, with a well-known thermal conductivity. This would allow the verification of conductivity data measured at each laboratory which takes part in a round robin test. Such round robin tests are required as there is no known set of reference materials which could be applied for the absolute calibration of the individual TIM testing solutions. This way each TIM testing system has to calculate the conductivity based on a number of individual parameters, and the associated error propagation is hard to define. Up to now the only way to achieve higher accuracy is to fine-tune the measurement of the variables shown in equation 1-1 up to the highest possible level and to verify the resulting conductivity based on results taken by other highly accurate TIM tester realizations.

Within the Nanopack project three individual round robin tests were carried out: at the beginning of the project over 100% scatter was identified among the test results obtained by the participating partners. By the middle of the project, the results of the second round robin test showed scatter below 30%. By the end of the project, a final round robin test showed less than 5% scatter among selected, high-precision test techniques.

This very well shows that creating an accurate TIM testing method and corresponding appliance is a very challenging task even for high level organizations, such as the members of Nanopack.

In the following section of my first research topic I present a newly developed methodology which was acknowledged as a high precision test method within the Nanopack project.
A new method for bulk thermal conductivity measurements [37,38]

Within the Nanopack project I have elaborated a measurement method that is based on the ASTM D5470 standard, but mimics the real application environment of the TIM. It also allows setting up the parallelism of the measuring surfaces as well as the distance between them. The method applies a power diode as heater/ temperature sensor element. A measurement following a similar principle can be done using any kind of semiconductor package with the appropriate cooling surface, if a uniform temperature distribution can be assured over the package face. In the newly developed setup the package of the diode is surrounded by a plastic thermal insulator; thus, the vast majority of the heat leaves the package through the exposed cooling tab. The heat-flow generated this way serves as probe for the TIM measurements.

In the new method the temperatures are not measured using thermocouples drilled in the heated and cooled rods, but at the junction of the semiconductor itself. An advantage of this method is that the TIM can be tested in its application conditions, one can apply pressure on the material and test the effect of particle congestions in the material matrix, making the measurement of ‘operation like’ thermal conductivity coefficient possible.

In the new arrangement the thermal interface material is put between the cooling surface of the selected package and a copper block that was directly mounted on a cold-plate. The distance between the cooling surface of the package and the metal block is set using a stepper motor in 1 micrometer steps. The accuracy of the BLT setting is maintained by the ratio of the fine angular movement of the motor and the width of the stationary screw that moves the semiconductor devices up or down along the rail. The equipment has a great mechanical stability to make sure that not only the resolution is fine, but accuracy of the set parameters is adequate as well. Possible error sources based on the mechanical flexibility of the system are carefully calibrated and corrected by software. The test arrangement can also be used to apply constant force on the sample.

By making a power step on the junction of the diode, the cooling curve describing the thermal system can be captured using a commercially available thermal transient tester. The cooling transients captured at different BLT values are turned into structure functions, which provide a map of the cumulative thermal capacitances of the heat flow path with respect to the thermal resistances measured from the location of the heating to the ambient. The schematic of the test system can be viewed in Figure 1-20.

Beside the partial thermal resistance values, the thermal resistance of the whole setup can also be measured with high resolution, which is the sum of the $\theta_{\text{total}}$ (see equation 1-2) and a thermal resistance characteristic to the measurement system. By subtracting the resistance of the measurement system from the overall thermal resistance ($R_{\text{thJA}}$), knowing $\theta_{\text{total}}$, the effective thermal conductivity can be derived using Equation 1-1, as the distance between the surfaces, the area of the cooling block and the power dissipation are known.
New methods for the investigation of modern packaging materials using thermal transient testing

For an accurate calculation however, the resistance of the TIM layer has to be separated from the resistance of the tester clearly. Unfortunately, even with the high resolution of the existing transient testers and the help of the structure functions, determining it with the required accuracy is extremely difficult.

In order to overcome this problem, I used a special ‘liquid metal’ alloy between the grips of the tester consisting of 62.5 Ga/21.5 In/16.0 Sn having its eutectic point at 10.7 °C, to measure the thermal resistance of the measurement system. This material has very high thermal conductivity and it is highly corrosive. By placing it between the metal surfaces of the cold-plate and the diode package, you can achieve a quasi-ideal thermal connection [39].

Figure 1-22 shows the structure functions measured on the silicon diode of the TIM tester at minimum BLT level using the liquid metal, and high conductivity thermal interface material at different thickness values. The notation of the curves serves as a reference for the TIM’s thickness, these are 600µm, 400 µm and 200 µm respectively, resulting in curves with lower and lower thermal resistance. The $R_{thJA}$ value of the liquid metal measurement is considered as the intrinsic thermal resistance of the tester, 0.69 K/W. This resistance point is indicated by a red marker in the graph.
New methods for the investigation of modern packaging materials using thermal transient testing

The perfect connecting effect of the liquid metal can be well observed as it creates an earlier separation point than the thermal grease applied in various layers shown in grey colors, as the corresponding contact resistance is about 0.148 K/W lower than the one corresponding to the thermal grease shown in the graph. The section between the two separation points is indicated by red arrows in the graph.

This $R_{\text{th}}$ of the test system is needed for the measurement of the effective conductivity of the TIM (the effect of the interfacial resistances included in the calculation) in the given environment based on one measurement point only:

$$k_{\text{eff}} = \frac{d}{(R_{\text{total}} - R_0)A}, \quad (1-8)$$

where $d$ is the distance between the grips of the tester, $R_0$ is the thermal resistance of the tester itself and $R_{\text{total}}$ is the sum of the thermal resistance of the sample, the contact thermal resistances and $R_0$.

Even though this way the proposed setup can take effective conductivity data, I focused on the measurement of the bulk thermal conductivity during this research. TIM material producers in most of the cases have no information about the exact application because it is different at each customer site. Yet they have to allow right comparison for their customers by reporting bulk thermal conductivity data of their materials.

The test setup also allows the measurement of the bulk thermal conductivity by varying the thickness of the TIM with high accuracy, see Figure 1-23. By plotting the resulting thermal resistance
values as a function of the distance between the measurement surfaces, the thermal conductivity of the TIM is inversely proportional to the slope of the resulting curve based on the following equations:

\[
k = \frac{\Delta L}{\Delta R_{th}} = \frac{1}{m} \quad \text{(1-9)}
\]

\[
m = \frac{\Delta R_{th}}{\Delta L} \quad \text{(1-10)}
\]

If you look at the measured thermal impedance curves (Figure 1-24) and structure functions (Figure 1-25), you can obtain useful information on the thermal performance of the setup at first sight. While the heat flow is inside the diode, both type of functions fit each other perfectly. As it leaves the package boundary, the functions start to diverge. The change of the thermal resistance of the system is directly proportional to the change of the thickness of the grease layer.

Knowing the \(R_{thJC}\) of the semiconductor package selected for the TIM testing application, any possible shift in the thermal parameters of the test system can be easily detected. If the structure functions describing the package match well until the \(R_{thJC}\) value, the tester’s performance is stable, however if the structure functions start to deviate at this early section, the results cannot be considered reliable anymore, as either the tester needs to be recalibrated, or the selected semiconductor package has started to degrade.

The junction-to-ambient thermal resistance is easy to be read from the structure functions using the vertical part at the end of each curve. In the measurement examples of the next chapter you can see thermal resistance values defined 10,000 Ws/K thermal capacitance on the structure functions, corresponding to each set BLT (see the red line in Figure 1-25).
New methods for the investigation of modern packaging materials using thermal transient testing

**Figure 1-24:** Measured thermal impedance curves at different BLT levels between 1 mm and 10 µm

**Figure 1-25:** Calculated structure function curves at different BLT levels between 1 mm and 10 µm
Measurements of different material types

Although determining the thermal conductivity based on the relationship between the thermal resistance and the varying bond line thickness is proven to be an accurate methodology, changing the material thickness is not always possible. For this reason, the ASTM standard differentiates three different material types. Based on the measurement experience gained during the Nanopack project, I would recommend the following three measurement modes for these distinct groups:

For Type I materials, such as *greases and pastes*, strict BLT control is recommended, without maintaining any pressure on the sample, assuming that due to its low viscosity, the excess material leaves the space between the grips as the BLT decreases during the test.

For Type II materials, *viscoelastic solids*, such as gap pads and gap fillers, BLT control with pressure limit is recommended, making sure that the material is kept at the target thickness. Setting up a pressure limit is important, so the system can identify the minimum achievable BLT. As this value influences the in-situ $R_{th}$ of the material, it should be listed in the datasheets.

For Type III materials, *non-compressible solids*, pressure control should be used. This way the measurement of different samples at different thicknesses is possible, assuming that the contact resistances remain the same due to the comparable pressure at each tested thickness. The use of a high conductivity thermal grease is recommended between the surfaces of the sample and the grips in order to keep the contact resistances stable and preferably at a low level. Keeping them stable is important to make sure that they cancel out at the conductivity calculation, and keeping them low is important to make sure that the heat flow can penetrate through the material to be tested and not re-directed by unnecessary airgaps.

In the following section I give measurement examples for each material type defined in the ASTM standard, and use stainless steel to prove the accuracy of the test methodology for TIMs having a conductivity coefficient even above 20 W/mK as it was defined in the research goals of the Nanopack project.

**Type I materials: greases and pastes**

The measurement of Type I materials is the most straightforward task, as the test system used in this research is designed for accurate BLT control. The BLT values used during the test should be selected such, that they correspond to the BLT range set in the targeted application. In this example the silicon based thermal grease was tested five times, the resulting test data can be viewed in Figure 1-26.
The average conductivity value based on the 5 subsequent measurements using 5 individual test systems resulted in 0.69 W/(mK) with a standard deviation of 0.02 W/(mK). The slight offset between the points corresponding to different measurements originates from the difference in the inherent thermal resistance of the different measurement systems. Due to the measured materials’ low viscosity, the excess material gets squeezed out from the gap between the tester’s grips, so no pressure was applied on the samples during the tests.

**Type II materials: viscoelastic solids**

The measurement of viscoelastic materials is a more complex task as their viscosity is much higher than the thermal greases', they do get compressed as the BLT is reduced during testing. Typical results measured on a viscoelastic gap-pad can be seen in Figure 1-27.

The mean value of the test results shown in Figure 1-27 is 3.45 W/(mK) with a standard deviation of 0.108 W/(mK). The corresponding pressure values range varied between 1000 and 1800 kPa. One can observe that the red and the green lines have an offset between each other. This can be explained by possible airgaps between the grips of the tester and the sample increasing the contact resistance at some measurement attempts. The offset however does not influence the slope of the curve, which is characteristic to the bulk thermal conductivity coefficient.
Beside the BLT controlled operation, pressure controlled measurement is also possible for the test of viscoelastic materials. This latter approach is widely used within the industry, as controlling the pressure is a more straightforward task than controlling the BLT in an application environment.

The mechanical behavior of such viscoelastic polymer compounds is described by the ‘Standard linear solid’ model, where the springs represent the elastic behavior of the model, while the dashpot models the viscous element of the material’s behavior. The model denotes that while a constant pressure is applied on the modeled material, due to its viscous behavior the thickness may change in time, see Figure 1-28.

By making pressure controlled measurements possible using the new test method, this behavior could be investigated.

![Standard linear solid model of polymer compounds](image)

**Figure 1-28:** Standard linear solid model of polymer compounds [40]

Figure 1-29 shows the drift in the TIM tester’s measured BLT as a function of time in three different pressure ranges, 1200, 2400 and 3600 kPa respectively.

![Measured BLT drift using the pressure controlled test mode](image)

**Figure 1-29:** Measured BLT drift using the pressure controlled test mode
The graph indicates that it takes the position app. 360 seconds to settle after the target pressure is set.

In a real measurement the case gets even more complex, as due to the temperature changes corresponding to the power cycles used, the mechanical parameters’ temperature dependence may play an increasingly important role.

Figure 1-30 demonstrates the effect of the pressure change, the heating pulse and the cooling section of the transient response on the measured position. The graph clearly indicates that the BLT of the material may not be constant during pressure control tests, introducing a possible measurement error.

On the contrary, the model shown in Figure 1-28 states, that the pressure may not stay constant if the measurement is conducted in a BLT controlled way.

![Figure 1-30: Position changes in a pressure controlled test, while the heating cycles are enabled](image)

Figure 1-31. shows the drift of the measured pressure while adjusting the thickness of the sample in 14µm steps at 250 sec intervals. Even though the material needs time to relax, the changing pressure should not influence the conductivity calculation.
The error introduced by the relaxation effect explained above obviously depends on the mechanical parameters shown in the model in Figure 1-28. The more elastic and the more viscous the material is, the smaller the error becomes. Figure 1-32 shows measurement data taken on a material where the error factor was not significant.

Although this example shows that the difference is marginal, close to the error limits of the individual measurements, the measurement mode in case of viscoelastic samples is advised to be chosen carefully.

**Type III materials: solids**

The measurement of solid materials may be important in a number of applications. Metals, ceramics, even adhesive samples cured between a sandwich of conductive layers should be tested
using this approach. The main difference to the previous two methods is that in case of Type III materials, even at higher pressures, no deformation should occur. For this reason, in order to maintain the ability to measure at different BLT levels, samples with different thickness values have to be prepared. A measurement example on AISI 422 grade stainless steel samples, with a textbook conductivity of 23.9 W/mK is shown in Figure 1-33. The goal of the test was to verify the accuracy of the test method at the target thermal conductivity range defined as one of the goals of the Nanopack project [41].

The sample thicknesses were varied between 3.5 mm and 1 mm in 0.5 mm steps. The resulting average conductivity data based on the four measurements shown above was 23.31 W/mK, with a standard deviation of 0.65 W/mK. This means 2.4% relative error for a solid sample in the targeted conductivity range of the Nanopack project to test high-end TIM materials.

![Figure 1-33: Measurement results on AISI 422 grade stainless steel samples](image)

The measurements were carried out such, that thermal grease was applied between the grips and the sample’s surfaces. The constant, 3.6 MPa pressure made sure that the grease is squeezed to an acceptably low BLT, and as all measurements were conducted using the same boundary conditions, the thermal resistance added by the grease cancels out [42,43] I have also found that if gap pad is used instead of the grease, the repeatability of the test results got worse.

The test does not only prove the accuracy of the method presented in my finding, but also shows that metallic samples could be good candidates to be used in round-robin tests, as they stay stable over a long time, their conductivity can be well characterized in bulk and due to their high conductivity the candidate measurement solutions can be compared in challenging conditions.

**Corresponding research projects**

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Finding 1.

I have elaborated a new methodology for the accurate and repeatable bulk thermal conductivity measurement of high performance (up to 20 W/mK) thermal interface materials. The new method combines the benefits of the currently accepted ASTM D5470-12 test standard and the benefits of thermal transient testing, without the need for using thermocouples. During the tests the thermal interface material to be measured is placed between the cooling surface of a power semiconductor package and a cooling block of similar surface shape, kept at constant temperature. By changing the distance between the two grips in fine steps and measuring the thermal impedance curve at each step, based on the obtained Rth vs. BLT function the thermal conductivity of a material can be clearly determined.

Finding 1.1

I have elaborated a methodology to obtain the $R_0$ value, the intrinsic thermal resistance of the test setup. In the new method, I use corrosive liquid metal to ‘thermally bind’ the grips of the tester, reducing the interfacial thermal resistance between the empty grips close to 0 K/W. Based on the difference of the thermal resistance measured with the sample placed between the grips and the $R_0$ value, the effective thermal resistance (including the effect of the interface thermal resistances) can be calculated based on the following equation:

$$k_{eff} = \frac{d}{(R_{total} - R_0)A}$$

where $d$ is the distance between the grips of the tester, $R_0$ is the thermal resistance of the tester itself and $R_{total}$ is the sum of the thermal resistance of the sample, the contact thermal resistances and $R_0$.

Finding 1.2

I have elaborated a methodology for the test of the structural integrity of the test system. The methodology is based on the fact that the $R_{jbc}$ (junction-to-case thermal resistance) of the power semiconductor component used in the tester is independent from the quality of the measured TIM material. This way each and every structure function obtained by the test system should overlap until the $R_{jbc}$ value. Storing a reference structure function taken after the calibration of the test system, and comparing it with the actual measurement data allows the identification of changes in the calibration of the tester, or structural defects in the power semiconductor used as a heater/sensor device.
References for research topic 1.

2. Nanopack Consortium: Nano Packaging Technology for Interconnect and Heat Dissipation, introductory video. URL: https://www.youtube.com/watch?v=HqtZf4MK-sA (last viewed 01.11.2017.)


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2. Research topic: A thermal transient testing based methodology to track the material changes and reliability of thin films and TIM materials

Abstract and research background

In my second research topic, a power cycling based in-situ reliability testing method is discussed for TIM materials. The material under test is put between the cooling surface of a TO-220 packaged semiconductor device and a cold-plate, resembling normal operation, while the whole assembly is fixed by a constant force. The heat is generated by powering the device in the package at the junction area. The generated heat is lead through the TIM into the cold-plate. The elevation of the junction temperature is used as a sensor to check the thermal property changes of the TIM. The heating power is cyclically switched on and off, and the junction temperature is measured after each cycle by a thermal transient tester. Slight changes in the junction temperature can be detected which correspond to the structural changes occurring in the heat-flow path. Structure functions are used to verify that the temperature changes originate in the tested TIM layer.

During the selection process of a TIM material, beside the bulk thermal conductivity value, the long-term behavior is also a very important factor. Within the Nanopack project the investigation of the lifetime of TIM materials was also a key task. The main goal of this research is to provide a tool which can monitor the changes of TIM performance after repeated reliability tests. Unfortunately, as discussed earlier, due to many physical problems testing of TIM materials is not a straightforward task [11,44]. Commonly accepted laboratory test methods such as transient thermo-reflectance measurement [45], direct thermal diffusivity measurement or the 3-omega method [17] are versatile and precise ways of characterization however they are not applicable for in-situ measurements. To characterize the TIM performance in each electronics application, e.g. to see the change of the thermal resistance value of a TIM layer after reliability tests, the measurements should be very fast in situ measurements with somewhat less demand for accuracy. As a powerful tool to observe any changes in the heat flow path the JEDEC JESD51-1 static electrical test method can be used [46] and enhanced by mathematical calculations; mapping over the heat-flow path from the electrically excited junction to the ambient by means of thermal resistances and thermal capacitances. In my second finding I combine the use of this tool with stress tests to track the lifetime of TIM-s in-situ.
A method to evaluate the quality changes of TIM-s, using thermal transient testing [47]

In the proposed test arrangement, the TIM material is put between the external cooling surface of a power semiconductor device and a heat-sink. The semiconductor is fixed to the surface of the heat-sink by constant force. This force is maintained by a simple fixture, as it can be seen in Figure 2-1. The highest temperature elevation and the total junction-to-ambient thermal resistance of the assembly are characterized at the device’s operating parameters to get reference values.

The first set of tests are aimed at the evaluation of the durability of TIM materials for temperature cycling, induced by power cycles. The temperature of the surface of the cold-plate can be set and maintained at any temperature between 5 to 100°C in the given experiment. The measurements are carried out with a thermal transient tester and its high power driving accessory. The high power excitation which results in temperature raise in the device is provided by the source. After reaching the hot thermal steady state, the high power is switched off and the cooling transient is measured by the transient tester. Such test conditions resemble the normal operation of the device: if the quality of the TIM gets worse, the same powering should result in higher junction temperatures in each cycle.

![Figure 2-1: The measurement setup for TIM reliability testing [48]](image)

May other failures occur in the device under test, the measurement results unfold them, too. As the resulting functions of the thermal transient measurements yield structural information of the whole cooling assembly, especially near the junction, beside the changes of TIM performance even die attach failures can be noticed this way.
To evaluate the above discussed test method, tests were conducted on 8 different TIM samples. As a heater element, a PNP type power transistor was used in TO-220 type package. The package was fixed on a cold-plate. The power step required for the measurements was generated using the so-called voltage step method [49]. A constant 2A current was forced through the open transistor, while the base-collector voltage was switched in 1 µs between -1V and -10V. Once the power step took place the base-emitter voltage was used as a temperature sensitive parameter to indicate the temperature response. The power step was 18.2 W, and the sensitivity of the transistor resulted in -1.1 mV/°C.

All measurements lasted for 20 seconds. It took 10 seconds for the junction of the transistor to heat up completely and another 10 seconds to cool down. In each test the samples were cycled for 2500 cycles, resulting in about 14 hours total measurement time.

The thermal behavior of 8 different, experimental TIM samples was investigated, however as most of them showed very similar results, only the most characteristic graphs are presented in this chapter. The list and composition of the TIM materials used for this study are summarized in Table 2-1:

**Table 2-1: List of thermal interface materials used in this study**

<table>
<thead>
<tr>
<th>Sample ID.</th>
<th>Filler</th>
<th>Matrix</th>
</tr>
</thead>
<tbody>
<tr>
<td>TIM-1</td>
<td>CNT</td>
<td>diluted epoxy</td>
</tr>
<tr>
<td>TIM-2</td>
<td>Al micro-particles</td>
<td>silicone</td>
</tr>
<tr>
<td>TIM-3</td>
<td>CNT + graphite</td>
<td>diluted epoxy</td>
</tr>
<tr>
<td>TIM-4</td>
<td>CNT + graphite</td>
<td>organic solvent</td>
</tr>
<tr>
<td>TIM-5</td>
<td>graphite + metal powder</td>
<td>resin</td>
</tr>
<tr>
<td>TIM-6</td>
<td>CNT</td>
<td>epoxy</td>
</tr>
<tr>
<td>TIM-7</td>
<td>silicone grease</td>
<td></td>
</tr>
<tr>
<td>TIM-8</td>
<td>CNT</td>
<td>epoxy</td>
</tr>
</tbody>
</table>

The surface temperature of the heat-sink was set to 40°C during all measurements. This allowed the junction temperature to rise to approximately 120 °C in each cycle.

To evaluate the results three views were used. The most straightforward way to see the difference between two measurements is to compare the transient responses. The transients should run together until the point in time when the main trajectory of the heat leaves the package boundary and enters the grease layer. The difference between the total elevations shows the change of the thermal resistance of the TIM material if no other structural element changes its thermal properties in the heat-flow path. Fortunately, this can be easily verified with the help of the structure functions.
Generated from the transient results using a mathematical procedure called the NID method [25], the structure functions represent the heat-flow path from the place where the power step takes place (so-called driving point) towards the environment. Both the thermal resistance of each structure in the heat-flow path and the thermal capacitance of the corresponding layer in which the heat spreads can be identified this way. Due to the high repeatability of the thermal transient method [27,50] as long as the heat flows in the same structure, the structure functions are exactly the same. If the structure of the heat-flow path changes the difference immediately appears on these functions, showing the exact location (thermal resistance value) and magnitude (thermal capacitance value) of the change. Hence with the help of the structure functions it can be made sure if it is really the TIM material which changes its thermal resistance in the assembly, or not.

As for each TIM material 2500 cycles were performed and the cooling transient for each cycle was captured, using the transient response - and structure functions only, their large number makes it very difficult to handle all of them together and to show clear trends. To overcome this problem, the temperature difference between an early point of the transient and the highest elevation was plotted after each measurement:

![Figure 2-2: Tendency of the final temperature of the junction using TIM-1](image)

Figure 2-2. clearly shows how the repeated power cycles make the thermal resistance of the TIM material lower and lower until app. after 500 cycles the material begins to stabilize. Along the x axis the number of the cycles can be followed, while the y axis shows the final difference between the temperature elevation at a very early time of the transient and the final temperature value.

The total temperature change during these cycles is app. 6.5°C in case of TIM-1. By plotting some transient curves and comparing them, this value can be directly read from the end of the curves.
The results indicate that the heat-flow path after the first cycle has the highest thermal resistance. After cycle 500 the TIM material becomes significantly better, only smaller changes can be seen later.

Figure 2-4 shows that the temperature difference between cycles 1 and 500 and above is already 4.5 centigrade.

The evaluation of the measured data after each cycle suggests that the TIM 1 sample is reliable on the long run even though it changed clearly in the initial 500 cycles, it just became better. This result also verifies the measurement arrangement. Applying this methodology, very small differences can be revealed in the heat-flow path. Moreover, the measurement itself is carried out with extremely high repeatability, as the temperature transient curves clearly fit each other up to 0.3 seconds.

In order to see whether the change is really caused by the TIM material’s property changes the structure functions have to be checked. Figure 2-5. shows that the structure functions generated by the transients of Figure 2-3 run together up to above 3 K/W, which is over the junction-to-case thermal resistance value of the transistor used for this study. This demonstrates that the structure of the heater transistor has remained unchanged, consequently the temperature drop is caused by the property change of the TIM layer.
Most of the tested materials (e.g. silicone grease) showed similar behavior, i.e. their thermal resistance decreased after the cycles. During the first 500 cycles, it can be assumed that the matrix rearranges itself, which results in lower contact resistance. After the first app. 500 cycles the change becomes less significant, the assembly is close to stabilization.

Some materials did not change at all, or the measurable change was close to the noise level.
Figure 2-6: Tendency of the final temperature of the junction using TIM-4

Figure 2-6 gives the tendency of TIM 4 material during 2500 cycles. Although some clear increase can be observed in the temperature up to 1000 cycles followed by a slight diminish, the maximum change during all 2500 measurements is less than 0.4 °C. Practically after finishing the test the junction temperature remains unchanged, the TIM 4 material is reliable. To make sure that the pattern on Figure 2-6 is not a summary of two effects, i.e. the change of the structure of the heater transistor plus the change of the TIM, it is worth to check again both the transients and the structure functions, see Figure 2-7 and Figure 2-8.

Very similarly to the TIM 1 material both functions are exactly the same on a large time and thermal resistance range. This indicates that during the measurement the structure of the transistor has not changed at all, the effect is characteristic to the TIM 4 material.
Beside decreasing and stable trends some materials also showed some minor degradation, at least in terms of thermal resistance. Materials TIM 3 and TIM 6 are good examples of this behavior. The slight degradation of TIM 3 during the cycles can be observed in Figure 2-9.

The behavior of the other materials also follows the tendencies shown before. For this reason, their graphs are not included, only the trends are listed in Table 2-2. Beside the trend (direction of the junction temperature change) and the cycle number of the stabilization, the maximum temperature changes are also listed.
Even though the temperature changes are not large during 2500 cycles, even the small changes can be measured very well. The resolution of the measurements is 0.02 °C in this measurement range, which is adequate for this purpose.

**Humidity testing using thermal transient test principles [51]**

As thermal transient tests have been proven extremely useful to observe material changes in-situ, I have extended my research to a slightly broader field to identify if they can be used for testing the humidity content in TIM layers. This can be useful in several applications, such as package hermeticity testing for MEMS devices, evaluating the results of HAST tests and in some special cases to measure the relative humidity of a gas.

It is a well-known fact that the relative humidity (RH) of the ambient atmosphere has a very low effect on its thermal properties such as thermal conductivity and thermal capacitance, especially at room temperatures, see Figure 2-10 [52]. At elevated temperatures, this effect gains higher importance, but it is still hard to detect the small changes of the mentioned parameters from thermal point of view [53,54].

**Table 2-2: Resulting trends and maximum temperature changes for TIM materials listed in Table 2-1.**

<table>
<thead>
<tr>
<th>Sample ID</th>
<th>Trend in Rth</th>
<th>Max. Temp. Diff. [°C]</th>
<th>Stabilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>TIM-1</td>
<td>decreasing</td>
<td>6,5</td>
<td>app. 1500, but still diminishing</td>
</tr>
<tr>
<td>TIM-2</td>
<td>decreasing</td>
<td>0,86</td>
<td>app. 2000, but still diminishing</td>
</tr>
<tr>
<td>TIM-3</td>
<td>increasing</td>
<td>1,1</td>
<td>app. 2000, but still increasing</td>
</tr>
<tr>
<td>TIM-4</td>
<td>increasing up to app. 1000 then slightly decreasing</td>
<td>0,4</td>
<td>stable, on the whole range within the noise level</td>
</tr>
<tr>
<td>TIM-5</td>
<td>decreasing</td>
<td>1,2</td>
<td>app. 1500</td>
</tr>
<tr>
<td>TIM-6</td>
<td>decreasing up to 150, then linearly increasing</td>
<td>0,78</td>
<td>no</td>
</tr>
<tr>
<td>TIM-7</td>
<td>decreasing</td>
<td>1,47</td>
<td>app. 250</td>
</tr>
<tr>
<td>TIM-8</td>
<td>decreasing</td>
<td>2,47</td>
<td>1000</td>
</tr>
</tbody>
</table>
A possible solution could be based on the fact that water has good thermal conductivity (0.58W/m∙K), compared to the air (0.0257 W/m∙K) and a relatively high specific heat of evaporation (2,25×10^6 J/kg). An encapsulated porous adsorbent material in the package under test may serve as a sensing layer. The humidity content of the porous layer, the rate of adsorption and desorption is highly dependent on the relative humidity inside the package. As the RH increases the number of the adsorbed molecules should increase and vice versa [55]. As the water fills the pores the overall thermal conductivity of the layer increases [56]. In case of high surface adsorbents, the decrease of the thermal resistance can be significant.

**Measurements in a HAST chamber, detection of humidity content**

One of the common environmental test for open packages and packaging materials is the HAST test. The definition of the HAST test is as follows:

*The Highly-Accelerated Temperature and Humidity Stress Test is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It employs severe conditions of temperature, humidity, and bias which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it.* [57]

The TIM samples selected for this tests were mounted in a similar way as described in the previous chapter, applied between the cooling surface of a power transistor and a cold-plate. The environmental conditions were set to T=135 °C, P=2 bar, RH= 100 % in the selected HAST test chamber. The devices were not biased according to the guidelines of the corresponding JEDEC standard during the test. As soon as the samples were taken out of the chamber, periodic thermal transient tests were carried out to see if there is any change of the $R_{thJA}$ of the system (which is the recommended failure criteria for such tests) as the humidity desorbs and evaporates from the structures.
Figure 2-11: Change of the $R_{th JA}$ of the selected transistors as the humidity leaves the TIM structure

Figure 2-11 show that the repeated thermal transient measurements can detect the change of the humidity content of the TIM, and show and the $R_{th}$ shows an increasing tendency as the material dries out.

Application of the method on porous materials [51]

**Proof of concept using gypsum as porous media**

In order to prove the applicability of high surface porous materials for sensing the moisture content, model experiments were carried out. A 0.1 mm wide gypsum layer was placed between a BD245C power NPN transistor in a SOT-93 package and an aluminum heat-sink. This type of transistor is designed to have a relatively small junction-to-case thermal resistance, 1.56 K/W according to the datasheet. Prior to the measurements, the gypsum was dried for 48 hours.

The transistor was used as a heat source in this measurement setup. The heat was forced through the gypsum layer into the heat-sink. Thermal transient measurements were carried out with the $T3Ster$ equipment to measure the thermal resistance of the gypsum at different moisture contents. The first measurement was made on the completely dry material; afterwards it was wetted with a small droplet of water. The same thermal resistance measurements were performed one after the other on the wet system.
The cumulative structure function (Figure 2-12) represents the heat flow path from the heated junction through the inner features of the SOT-93 package and the gypsum layer at different moisture contents into the heat-sink. The measured structure shows the highest junction-to-ambient thermal resistance (measured between the origin and the singularity point where the function goes to the infinite thermal capacitance values) when it is completely dry. The lowest junction-to-ambient thermal resistance value is shown when the structure has the highest moisture content, right after wetting it with a water droplet. The structure functions between the two states were measured one after the other with app. 2 minutes differences. As the humidity evaporates from the structure, the partial thermal resistance of the gypsum layer increases. The diverging point of the cumulative structure functions (indicated at 1.78K/W in the image) gives a good estimation for the junction-to-case thermal resistance of the package, in other words until that point the heat propagates inside the package, after that point the heat propagates through the gypsum layer [58]. Using -2mV/K for the sensitivity of the silicon device, this point is very close to the 1.56 K/W value obtained from the datasheet of the transistor.
A porous silicon based micro device [58,60]

As the effect of the RH changes of the air on its thermal conductivity is too small to be measured directly with thermal transient measurements, a methodology had to be found to enhance it. The application of high surface porous materials is a possible solution. The thermal conductivity of porous materials is highly affected by their porosity. If they are in dry environment and 0% RH, the pores and cavities inside their structure contain dry air only. As the air has a low thermal conductivity the overall thermal resistance of the structure is large. At low RH levels the water molecules from the gas phase start to adsorb on the wall of the pores and cavities. As the RH increases more and more layers of water adsorb on the pore walls until at a certain RH level capillary condensation occurs [56]. As the water is a more than 20 times better heat conductor than the air, the overall thermal resistance of the layer decreases with the increasing humidity content. In many cases the moisture can penetrate the pores from liquid phase as well, causing the same thermal effect.

Based on the experiences gained of the macro-scaled test assembly, a microstructure was used to evaluate the applicability of porous materials for package hermeticity testing. The analyzed heaters and temperature read-out elements consist of Pt resistor filaments embedded in silicon rich silicon-nitride. The reduced stress silicon-nitride is deposited by LPCVD process. The micro hotplates (100×100×1µm³) are suspended across a 60–80µm deep, electrochemically etched porous silicon sensing layer [58,61].

The microstructure was exposed to various RH levels. In order to set and maintain such RH conditions, the closed environment over saturated salt solutions was used. Following the fixed-point RH sensor characterization methodology, MgCl, NaCl, KCl, KNO₃ solutions were applied to set 4 different RH levels, 32.78%, 75.29%, 84.34%, 93.58% respectively [62]. The temperature of the test environments was maintained at 25 °C by a water-cooled thermostat.

Cooling transient measurements were carried out. A sensor current source was used to maintain a small but well measurable threshold voltage on the platinum heater. The driving current source can be switched on and off very quickly in 1 µs to produce the power step excitation of the Pt meander. The fast switching is obtained by keeping the sensor current always on and redirecting the driving current from the sample to a shunt suddenly using fast switches, such as MOSFET-s with low serial resistance. This way distracting Voltage kicks induced by the reactive components of the circuit can be eliminated.
The temperature induced voltage change of the Pt resistor is measured and recorded continuously by the measurement channels of the T3Ster, see Figure 2-14. This real transient was evaluated and transferred into other system descriptive functions by the T3ster-Master software tool.

The driving current source was also used to heat up the sensor devices after each change of the RH environment, in order to make the adsorbed water molecules evaporate from the porous structure and to set the output offset of the sensors.

![Figure 2-14: Schematic of the measurement setup](image)

Since the most important sensor response is the thermal conductivity change of the porous adsorbent layer, the thermal transient measurements were stopped before reaching thermal equilibrium. Each measurement lasted for only 500 ms, which is sufficient to characterize the porous silicon under the Pt heater, but not enough to consider the thermal effects of the whole package.

The resulting temperature response curves are shown in Figure 2-15. The highest temperature value was reached at low RH environment corresponding to the best thermal isolation of the heater structure. The final temperature reached in transient regime strictly decreases with raising RH, indicating an improvement in the thermal conductivity of the porous layer. The difference between the highest and lowest values resulted in 2.54 °C, in this particular case.

![Figure 2-15: Temperature response curves of the porous microstructure at different RH levels](image)
The transient curves run together until app. 30 µs, indicating the characteristic time of the heat propagation from the source to the porous layer along the main trajectory of the heat flow in the heater structure. As the front of the heat reaches the porous silicon with different humidity contents, the functions start to diverge. The heat flow path in the sensor structures can be reconstructed using the structure functions. Note that the interpretation of the structure functions is not straightforward due to these were not generated from steady state – to – steady state transient responses. However, the results provide valuable information about the first structural layers of the sensor device, including the app. 60-80 µm thick porous silicon.

The highest thermal resistance between the Pt heater and the bottom of the porous layer (bulk silicon) was measured in the driest environment and the thermal resistance of the layer diminished as the surrounding relative humidity content increased. These functions can be used as humidity – proportional output of a possible package hermeticity tester.

Figure 2-17 presents the comparison of the time constant spectrums of the devices at the highest and lowest humidity levels. The second peak corresponds to the main time constant of the porous layer. The intensity value of the given time constant in the spectrum is proportional to the actual thermal resistance of the active layer affected by the surrounding humidity and observed higher at low RH level (KNO₃ solution).
It is important to note, that there is a time shift between the two peaks relating to the thermal capacitance change of the layer as the consequence of the water content of the porous layer. However, this effect is rather small, it could open further opportunity to estimate the absorbed amount of water in the porous matrix.

**Simulation of the thermal behavior**

The package hermeticity testing methodology was also evaluated by thermal simulations using the Sunred software which is based on successive network reduction [63]. A scaled model of the sensor structure was built including the porous silicon layer with a number of artificially designed pores. Both steady state and transient simulations were carried out in order to show the difference between two extreme conditions, empty pores and pores filled with water.

In all simulation cases the ambient temperature was set to 0 °C, this way the simulated absolute temperature value and obtained temperature change is the same. I could do this simplification as the simulator software did not take the temperature sensitivity of the material parameters into consideration. If it did, using the real ambient temperature would have been necessary. The transient simulations were started at 1μs and the time sampling was logarithmic. The simulation results were compared to the results of the measurement on the same structure.

The simulation results of the porous silicon based micro testing device showed very good correlation with the measurements. The result of the steady state simulations of the built thermal model (see fig.8), in case of empty pores and in case of pores filled with water showed significant difference between the two investigated cases. In case of dry pores the highest temperature elevation was 25.42 °C while in case of wet pores the elevation dropped to 24.13°C.

The results of the transient simulations were also similar to the measured curves. The two transient responses started to diverge at early times, app. at 100 μs, which should be the time constant of the porous sensing layer and the heater element together. The transient curves were
once again turned into structure functions, see Figure 2-19. These derived functions show that in the region of the heater the curves run together and start to diverge as the heat enters the porous layer. The heater region shows a very high thermal resistance, which is true as the heat cannot spread well on the suspension of the heater element, only through the porous structure. In case of the structure functions of the measured curves this region is smaller, probably due to some physical effects which were not simulated, e.g. natural convection.

**Figure 2-18:** Thermal model of the microstructure on the left and the temperature distribution of the platinum filament on the right. The warmest point is 24.13°C

**Figure 2-19:** Structure functions generated from the simulated transient response. The graph indicates the decrease in the thermal resistance due to the moisture elevation

This approach could be used for the measurement of the RH content of a gas mixture in equilibrium, however to do so, an additional calibration step would be necessary. This could be carried out in an environment where various fixed RH points can be set, such as an environmental test chamber. The calibration should be done using both increasing and decreasing RH points, to see any possible hysteresis. The calibration of the sensor was not part of my thesis; hence it is not described here in more details.

**Corresponding research projects**

This work was supported by the PATENT IST-2002-507255 Project and NANOPACK FW7 No. 216176/2007 IP Project of the EU and the SE2A ENIAC Joint Undertaking Project of the EU No. 12009.
Finding 2.

I have elaborated a new methodology for testing the long term stability of highly conductive thermal interface materials.

In the methodology, the material to be tested is applied between the cooling surface of a power semiconductor device and a cold-plate. Aging of the TIM occurs by periodical powering of the semiconductor die and is tracked by thermal transient responses measured in the die area. The strength of the methodology is that the structure functions calculated based on the measured transient responses can be used to identify the physical location of the degradation in a complex, multi-layered system.

Finding 2.1
Using the new methodology, I have demonstrated that in case of thermal greases and pastes the thermal cycles induced by the continuous power change may increase the effective thermal conductivity of the TIM, as the cyclical temperature changes allow the material to spread between the matching surfaces better, resulting in lower thickness and/or interfacial thermal resistances.

Finding 2.2
I have demonstrated, that the HAST tests used widely in the industry as a standard environmental test (135°C, 2 bar, 100% RH), may fill up the TIM matrix and the voids between the TIM and the matching surfaces with humidity, temporarily increasing the effective thermal conductivity of the tested material. I have shown that the presence of the humidity and the drying process can be tested using thermal transient test method.

Finding 2.3
Based on the results shown in Finding 2.2 I have elaborated a new methodology to measure the humidity level of porous layers using thermal transient test methods. Following the pattern of the above introduced method, the layer to be tested is put between a heat source (power semiconductor package, resistor, etc…) and a cooled surface, assuring that the tested layer is part of the main heat-flow path. The humidity content of the layer is inverse proportional to thermal resistance, which can be accurately tested this way.

Finding 2.4
Using experimental methods, I have demonstrated that the measurement method proposed in Figure 2-1 is also applicable for the measurement of the relative humidity of gas mixtures, if a proper porous sensor layer is selected. I have proven experimentally that the thermal resistance of a porous silicon oxide layer located beneath a micro-meander heater changes as a function of the relative humidity of the environment.
References for research topic 2.


52. Tsilingiris, P.T., "Thermophysical and transport properties of humid air at temperature range between 0 and 100 C", Energy Conversion and Management, 49, 2008


57. JESD22-A110-B Standard, “Highly-Accelerated Temperature and Humidity Stress Test (HAST)”, February 1999


3. **Research topic: A methodology to refine the model parameters of multi-layer numerical package models based on thermal transient test data**

**Research background and motivation**

As the functionality of thermal simulators gets more and more complex, measurement techniques also improve. Thermal engineers face and increasingly difficult task to make the right selection from the existing tools. In this section the applicability of the JEDEC JESD 51-1 static measurement method is introduced to support mainstream simulation tools, especially MCAD or EDA embedded CFD (Computational Fluid Dynamics) solutions.

The most important data provided by thermal characterization tools are the different standard thermal metrics of semiconductor devices, such as $\theta_{JA}$, or $\theta_{JC}$, etc. For this reason, there is an emerging demand from system level designers on simple, fast and preferably standardized methodologies that are capable to provide these and allow proper prediction of the junction temperatures quickly and accurately. Using the existing standards and developing new ones is essential in order to put consistent thermal results in the datasheets of such devices. Besides the usual thermal metrics of packaged devices, nowadays compact thermal models such as the JEDEC-2R or DELPHI style models are also often required.

In case physical testing of semiconductor packages (besides IR thermography) the mainstream characterization technique is based on the JEDEC JESD51-1 electrical test method, yielding either thermal resistance values only (see e.g. [65], [66]) or providing the dynamic description of the packaged multi-die system by means of thermal impedances in various forms (see e.g. [67] or [68]). Thermal transient measurements are mainly used to derive steady-state metrics for multi-die systems [69] though so far there exist no standardized thermal metrics e.g. for stacked die packages or other multi heat source systems. In case of all above mentioned measurement techniques the evaluation procedures are based on real time data acquisition. The physical time required for the measurements – even in the most optimal case – is determined by the thermal time constants of the device under test. Depending on the size of the DUT and the thermal boundary conditions (thermal environment) this time varies between ~30s and ~30 min, or maybe, a few hours (if a large device is measured in natural convection environment).

On the other hand, a wide choice of simulation tools available, applying different methodologies. In case of finite element methodology (FEM) usually only the heat conduction is taken into consideration. Computational fluid dynamics (CFD) simulators are capable of characterizing a wider range of thermal environment enabling the user to simulate the package with its cooling assemblies and PCB or even to model the airflow properties within the electronics box. However, the application of such tools requires high proficiency and modeling experience from the thermal engineer’s side.

The greatest challenge of thermal simulations is the creation of the thermal model itself. Complex geometries are in most of the cases are hard to build, so the engineers have to consider
simplifications which do not corrupt the simulation results. Integrated solutions in EDA environments usually support automatic thermal model creation from an already existing detailed geometrical model. The modeling of the real world has become possible this way. Unfortunately, these methods have their drawbacks as well. You can save precious time on the model creation, however even to carry out a DC simulation of such a complex model may take much time.

Weighing the above-mentioned factors thermal designers need to decide which method suits their needs the best, which consumes less time. Unfortunately, there are also cases when automatically building a correct thermal model is impossible even in an integrated EDA environment – mainly due to the unknown thermal properties of thermal interfaces.

In real structures the quality of the heat flow path strongly depends on the quality of the thermal interface layers. In relatively simple case such as a power IGBT there are multiple such interfaces as shown in Figure 3-1.

![Figure 3-1: Different thermal interfaces in the junction-to-ambient heat-flow bath of a power IGBT](image)

Especially, the different solder or sintered metal layers play an important role in case of power transistor assemblies, where the main cooling mechanism is heat loss by conduction. Unfortunately building a correct model of such layers is in most of the cases extremely difficult due to many unknown physical parameters such as the roughness of each layer, possible air bubbles in thermal grease layers, cracks or voids in die attach layers.
New methods for the investigation of modern packaging materials using thermal transient testing

Calibration of the thermal properties of TIM layers in a power transistor package model based on measured data [70,71,72]

In this section a novel methodology is investigated to create accurate thermal models without having validated information on the effective thermal conductivity coefficient of the applied thermal interface materials. The calibration of the detailed numerical thermal model is based on the physical information which can be derived from experimental structure functions. I will demonstrate a complete calibration procedure using a TO-220 package as an example.

For the comparison of the simulation results with actual measurements a TO-220 power transistor package was selected. As a first step a ‘best guess’ 3D numerical model of the package and the characterization environment was created.

The package hosts a simple BD-242 type transistor and the geometry was built up based on measurements. After the thermal tests the mold compound was removed and the package features’ geometry was measured manually. The package (X,Y,Z) and die (X,Y) sizes are quite easy to identify as are, to a lesser extent, the metallic material properties, however the bond-line thickness and the thermal conductivity of the die attach layer is difficult to measure. Please note that these values are normally given for a package design engineer.

During the thermal characterization, the sample was pressed against a water-cooled cold-plate while thermally conductive grease was used to establish proper thermal contact between the diode package and the surface of the cold-plate. The numerical simulation was conducted by FloTHERM from Mentor Graphics. Convective and radiative heat transfer were assumed insignificant and thus not modeled. The circulated water was modeled as a region of constant temperature.

As a first step thermal transient measurements were carried out on the packaged semiconductor device. Thermal transient measurements require a power step on the junction of the semiconductor device, which is usually supplied by electrical means. In this measurement, the following electrical setup was used:
Before the actual measurement starts, the sum of a heating current and a measurement current is forced through the semiconductor device. As the temperature of the diode stabilizes the heating current is suddenly switched off. Typical fall time is less than a 1µs. As soon as the switching takes place from the high current to the measurement current value, the voltage of the device is monitored with a time resolution of 1 µs and a voltage resolution of 12 µV. The measurement starts at the switching and finishes in the cold thermal steady-state of the diode as prescribed by the JEDEC JESD 51-1 test standard. Based on the voltage change of the semiconductor it is easy to calculate the temperature change knowing the so-called k-factor, the relationship between the diode’s forward voltage and the temperature at a constant, steady current. The sensitivity measured on this diode was equal approximately to the textbook value, 2.15 mV/°C. Knowing the k-factor and having the temperature vs. voltage characteristics measured by the transient tester it is easy to plot the change of the junction temperature of the device during the test.

The power step used in this study was app. 5.45 W. For comparison purposes the same power was set in the thermal simulator to the active volume of the silicon die. For ease of simulation, the numerical model considered a step increase in power dissipation. Both the measured and simulated temperature difference curves can be viewed in Figure 3-4.

Even though the number of the “bumps” in the curves is similar, the temperature elevations over time show a different behavior. Important unknown parameters in the detailed model are the thermal conductivity and bondline thickness of the die attach layer and effective thermal conductivity of the grease at the package boundary (including the interfacial thermal resistance value).
New methods for the investigation of modern packaging materials using thermal transient testing

In order to identify the source of the differences between the curves in Figure 3-4, the transient responses were turned into system descriptive structure functions [25,73].

In the structure functions the cumulative thermal capacitance is plotted as a function of the cumulative thermal resistance. If the heat-flow path is mainly one-dimensional, as in the case of most power semiconductor packages having an exposed cooling tab, these functions provide a map of the heat-flow path from the heat-source which is the semiconductor junction to the ambient. This approach allows the identification of partial thermal resistances and partial thermal capacitances in the main heat conduction path.

The structure functions corresponding to the measured sample and the detailed model can be seen in Figure 3-5.

When comparing a simulation to a measurement these graphical structures may help to identify the source of the difference between two results in terms of which package structures are responsible for the observed differences. This is impossible to be done by analyzing the time-domain curves only. In case of comparing a simulation to a real measurement this approach may help to fine-tune the simulation model by revealing material property data of the internal layer structure.

In order to ‘calibrate’ the detailed numerical package model one has to refine the measured geometry and material parameters that way that after re-running the simulation the calculated structure functions get into a better alignment with each-other. In the current study this was done in a systematic way starting from the die.

Figure 3-4: Measured and simulated transient responses of the studied structure

![Graph showing measured and simulated transient responses](image-url)
As a first step the die capacitance was identified based on the measurement based structure function. It was clearly lower than the one calculated based on the simulation model.

In order to calibrate the part of the structure functions describing the die, its capacitance can be calibrated by modifying the following numerical model attributes:

- Die size
- Die thickness
- Active layer thickness (can be assumed as ~ 2 to 5 microns)
- Active layer coverage (sometimes due to die slicing this can be between 100-150 microns smaller from each edge of the die area)
- Silicon density and specific heat

In the current case the die volume had to be reduced to achieve the measured 0.14 J/K value. To achieve good match beside the die area (due to incorrect measurements at the beginning), the active area coverage had to be reduced as well.
After making the changes shown in Figure 3-6, we found that active area size reduction helped reduce capacitance to correct level and increased resistance causing good fit right up to 2.35 K/W, see Figure 3-7.

The next step towards perfect calibration is to identify the location of the error point on the numerical structure function, i.e. where it deviates from experimental structure function in terms of resistance value.

The following calculation was used to identify where spatially in the simulation model the deviation occurs:

\[ R_{thX} = \frac{T_J - T_X}{Q}, \]  

\[(3-1)\]
Where $R_{th}$ is the thermal resistance from the junction to the point of the deviation, $T_j$ is the junction temperature and $T_x$ is the temperature of the given point (rather the thermal iso-surface at that value). $Q$ stands for the heat flow from the junction. $Q$ should always be the total input power as the structure function theory assumes an essentially 1D heat-flow.

The area in the model at this resistance can be visualized using a iso-surface or clipped temperature plot at

$$T_x = T_j - (R_{th} \times Q),$$  \hspace{1cm} \text{(3-2)}

where $T_x$ equals to 30.34 °C in the current case.

According to the results shown if Figure 3-8, the spatial location of the error is in the spreader beneath the die attach. This is where the temperature is at the required value as well as being on the heat conduction path as opposed to the area above the die that is not on the dominant conduction path. This suggests that no modifications have to be carried out in the die attach numerical model, but the heat-spread material was defined imperfectly. The spreader area clearly seen on the experimental structure function, the steep section is typical to source spreading in metal.

The corresponding numerical model is both too resistive and not capacitive enough. If the numerical structure function was rotated anti-clockwise, that would give a better fit for the spreader.

After a detailed investigation of the simulation model used, it was revealed that the spreader material was not correctly defined. In order to change this the ‘correct’ material was attached to the flag, i.e. the spreader material was changed to $\lambda = 301$ instead of $\lambda = 188$ W/mK. The 301 W/mK value corresponds to a special copper alloy, called CU-EFTEC-64T, so it is a realistic result.
After these changes the matching is still not perfect. It appears that there may still be a small misalignment in the die attach thermal resistances. This can be proven by the fact that by shifting the numerical structure function to the right you can get perfect match at the heat-spreader region. The magnitude of the shift in terms of thermal resistance gives the fixed $R_{th}$ value which should be added to the die attach thermal resistance by changing its material properties. In this case this fixed resistance value was as small as 0.1 K/W. The corrected curve can be observed in Figure 3-10.

As a final step the thermal resistance of the TIM2 material had to be aligned. Unfortunately, this correction cannot be done by simply adding the missing thermal resistance to the TIM2 layer in the numerical model. The reason may be that the heat-flow in case of this model in the studied region is not essentially 1D anymore resulting in a smoothing of the structure function gradients. At this late stage on the structure function the only action is to do a trial/error iterative simulation approach. After the modifications in TIM2, the final result can be seen in Figure 3-11 below.
The approach to calibrate numerical package models using experimentally derived structure functions allows packaging engineers to build accurate models without the knowledge of the real material property values of thermal interface materials in the system. This approach however requires a deep understanding of both the thermal transient testing technology and the CFD simulation methods. The main benefit of the methodology is its applicability on a wide range of packages [74,75].
Correction of the effect of initial electric transient response on a thermal transient test using CFD simulation [76]

Due to the power step forced on the sample during thermal transient testing, each measured curve starts with an electric transient section. In case of two-pole devices the power change is realized by switching between two current levels, a so-called driving current and a sensor current. The progress of current and voltage changes during a thermal transient measurement are demonstrated on a typical I(V) curve of a diode in Figure 3-12.

![Figure 3-12: Powering sequence for a thermal transient test](image)

Point 1 represents the initial state with only the sensor current applied to the diode at a reference temperature (cold state). First the driving current is switched on and the voltage jumps to point 2 according to the blue characteristic. The driving current heats up the junction, and when a thermal steady state is reached (point 3) the power step is realized by switching back to sensor current level, see the transition between points 3 and 4. This way the device is switched from one operating point to another, which results in a sudden drop in the device voltage following the red line, the characteristic curve of the hot device. This is the electrical transient which lasts normally from 10μs in case of small devices up to 100μs in case of larger power devices. After the power step the device starts to cool down, however in the early times the electric transient covers the temperature induced voltage change, which would be the real area of interest. Ideally the thermal transient should be known from t=0 sec, so methods have to be elaborated to retrieve or at least approximate the missing signal. This effect may cause more significant error in case of large area VLSI IC-s or solar cells, however for the more accurate $R_{thJA}$ or $R_{thJC}$ measurements the accurate identification of the missing thermal response is a crucial task in case of each and every thermal transient measurement [77]

The physical reason of the initial transient is purely based on electric background. Each PN junction has parasitic capacitances which have to be charged or discharged at each and every power step. One can differentiate between diffusion and junction capacitances. Diffusion capacitance has
only influence in the forward domain of the diode. Due to the forward current, charge carriers are injected to the p region, accumulating electrical charges there. The accumulated charges form the diffusion capacitance, the amount of charge carriers stored are forward current dependent, which shows capacitive behavior.

The junction capacitance has effect in both forward and reverse direction. The width of the depletion region of the PN junction depends on the actual voltage powering the device. As the voltage is changing, the width of this region is also changing; charge carriers are injected and removed accordingly.

In case of a thermal transient test the device is switched from a high current operating state to a low current operating state, which induces the capacitive behavior of the junction. The charge and discharge of these capacitances induces the electric transient response, which cannot be dealt with experimentally, therefore numerical methods have to be elaborated.

One common approach is to find the end of the electrical transient and substitute it with a constant which goes back to t=0. Another approach (described in the JESD51–14 JEDEC standard) is to fit a square root function to the beginning of the curve, which gives a higher, more realistic temperature rise function. This can be done as if the surface of an infinitely large, uniform material is heated by a power step, the temperature rise of that material surface will be proportional with the square root of the heating/cooling time [29,78].

\[
\Delta T(t) = \frac{P \cdot k_{\text{therm}} \cdot \sqrt{t}}{A},
\]  

(3-3)

where \(P\) is the heating power, \(A\) is the area of the chip and \(t\) is the heating time, and

\[
k_{\text{therm}} = \frac{2}{\sqrt{\pi \rho \lambda}},
\]  

(3-4)

where \(c\) is the specific heat, \(\rho\) is the density and \(\lambda\) is the coefficient of thermal conductivity.

This type of correction is valid only for the beginning of the curve, while the heat spreads in the chip. There is in all cases a maximum time point above which this approximation will not be valid any more. This mostly depends on the thickness of the chip:

\[
t_{\text{valid}} = \frac{d_{\text{chip}}^2}{2\alpha},
\]  

(3-5)

where \(d\) is the thickness of the chip and \(\alpha\) is defined as

\[
\alpha = \frac{\lambda}{c \rho},
\]  

(3-6)
Another simple, but commonly used method to deal with the electric transient is the use of a constant fit from the first point of the transient response which bears thermal information to the origin. The difference between the two methods in terms of junction temperature can be several percent, see Figure 3-13. The square root method gives more realistic junction temperature value, while fitting a constant to the beginning of the curve is a more repeatable approach. It is advised for comparison between many measurements.

![Figure 3-13: Initial Transients Approximated Using Square Root Fitting and Minimum Seek Methods](image)

After the calibration process introduced in the previous chapter, one can be sure that the simulated thermal transient response of the model is a good approximation of the measured thermal transient. In this case it can also be assumed that the early section of the simulated thermal signal that is covered by the electric transient in the measurement is also a good approximation of the real temperature change. So by substituting the early section of the measured curve with the simulated transient a better initial transient correction can be achieved.

In order to be able to create a combined transient you have to find the appropriate point to join the two curves. It is given that the thermal transient and its derivative is a continuous function. The combined function also must be continuous, thus the time point has to be found, where the derivative of the measured and simulated transients is equal. This simple task had been solved by numerically finding the minimum of the difference of the derivative functions.

Calibrating the detailed model of the whole device is an iterative, time consuming procedure. Moreover, the simulation time is also highly dependent on the model complexity while for electric transient correction it is enough to use the initial section of simulated transient, which is normally below 100 µs. The structural elements far from the junction affect the thermal transient only after a certain time delay. This effect was investigated by removing model elements from the above introduced package model starting from the far area of the die, one by one, and running transient simulations for each case. In Figure 3-14 the transients of the whole calibrated structure (blue), after removing the cold-plate (red), the TIM material (black), heat spreader (green), the die-attach material (brown), and finally modifying the area of the active surface (yellow) can be seen.
You can observe that even removing the closest layer, the die attach, the transient response remains unchanged until about 200 μs, which is about 100 μs longer than the end of the electric transient. This gives the possibility to significantly reduce the model used for the simulation based early transient correction and also to reduce the length of the simulated transient, decreasing the time spent on the simulation significantly as well.

As a result of the model reduction the time-consuming calibration process no longer has to be performed. The model contains only the die itself and the active region. Only the thermal parameters of the die material (thermal conductivity, specific heat) and the geometrical parameters shown in Figure 3-15 have to be known. The importance of the size of the active region has to be highlighted in this application. In most of the cases the whole chip surface is not entirely covered by the dissipating element and this can significantly affect the shape of the initial transient.
**Example structures – a TO-220 packaged power transistor**

The TO-220 packaged transistor from the previous study was selected as the first demonstrator of the methodology. The size of the die was 1.3×1.3×0.3 mm. Based on preliminary experience the active region was selected to be 1.1×1.1 mm, due to a 100μm wide undoped region along the edges. In Figure 3-16 the measured (black) and simulated (red) transients are shown. The two transients fit well in the time range between 75 μs and 350 μs indicated by the vertical markers.

![Figure 3-16: Measured (black) and simulated (red) transients corresponding to the transistor package in Figure 3-2](image)

A square root function has also been fit to the section between 75 and 350 μs and plotted with black dashed line in Figure 3-16. The initial transients calculated using the square root method and the one determined by simulation fit perfectly, demonstrating that the two methods give consistent results if proper parameters are applied.

**Example structures – solar cells with larger active area [79,80]**

The effect of the electric transient is higher in case of large area semiconductor devices, such as solar cells or VLSI IC-s, therefore finding a correct fit becomes more important.

Figure 3-17 shows a thermal transient measurement of a solar cell including the initial electric transient.
In order to identify the length of the electrical transient depending on the geometry and electrical biasing, GaAs concentrator solar cell samples (CSC) of different sizes, mounted on an aluminum based MCPCB were prepared for thermal test purposes. The structure of the samples is shown in Figure 3-18 is similar to those used in case of power LED-s, therefore one may assume that the heat-conduction path is mainly one dimensional in this particular case.

During the tests we have observed that the initial electric response may significantly differ among different samples and test conditions.

<table>
<thead>
<tr>
<th>Sample size [mm]</th>
<th>Electric transient length [µs]</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 x 10</td>
<td>22</td>
</tr>
<tr>
<td>20 x 20</td>
<td>79</td>
</tr>
<tr>
<td>20 x 30</td>
<td>129</td>
</tr>
</tbody>
</table>

Comparing the electric transient length measured on samples of different size, you can observe that the length of the electric transient increases with the surface area of the sample, see Table 3-1.

The effect of the measurement and heating current on the transient length was also investigated. Generally, with the increase of the measurement current the electrical transient length
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decreased. The increase of the heating current however has an opposite effect, higher heating current levels result in increasing electric transient length, see Figure 3-19

![Figure 3-19: Length of the electric transient as a function of the measurement and heating currents](image)

Even though the tendencies shown in the figure appear clearly in all cases, from the aspects of the measurements the electric transient length is not influenced significantly. However, as the increase of the size of the solar cell results in longer electric transient responses, in case of large area cells a significant part of the thermal information may be covered by the parasitic effect. One can conclude that the proper selection of the measurement and heating current levels may reduce the length of the electric response, however due to the relatively low sensitivity, if this method cannot lead to sufficient results, the simulation of the early part of the temperature response may be a suitable solution.

One of the differences between this and the previous example is that the active area of the die is unknown, so in order to achieve suitable fit between the die and the package area, in this case the entire thermal structure of the solar cell was also calibrated.

As mentioned above, the most challenging structures to simulate are the thermal interface materials as often both their thermal conductivity and bond-line thickness are unknown parameters. Stable structures, which are easy to model, can be the silicon itself and the underlying metal base. The resistance of the die-attach layer has to be calibrated separately by tuning its material parameters until the best fit with the measured curve is achieved both in the time and the structure function space.

The detailed numerical model of the simulated sample can be seen in Figure 3-20.
At the creation of the numerical model the geometry was built up with the highest precision and most of the material parameters were known. Still it took 14 iterations to refine the model that way that the simulated transient response matched the measured one with a satisfying accuracy. Major alignments were done at both TIM layers. The resulting transient responses can be observed in Figure 3-21, and the early section of the cumulated structure function describing the cell, the die attach and the copper base-plate regions can be observed in Figure 3-22.
As it can be seen in the figures above, the simulation resembles the original measurement results well, except for the early sections of the curves. The difference in the part of the structure function describing the solar cell is caused by the correction used to substitute the initial electric transient, that was applied in case of the measured response. As all sections except for the one describing the solar cell fit well, we may assume that the simulation has been correctly calibrated for the structural elements of interest. From this one can conclude that the thermal information covered by the long electrical transient can be regained using proper simulation techniques. The prerequisite of this is the thorough calibration of the model to well-known elements in the assembly, such as the chip and base plate material and geometry.

**Corresponding research projects**

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Finding 3.

I have elaborated a methodology for the refinement of material parameters and layer thickness values for simulation studies. The methodology relies on the iterative comparison of a structure function calculated based on the transient simulation results of a detailed package model with nominal parameters, and a structure function calculated based on thermal transient measurements taken on a real physical device.

Finding 3.1
- In the new methodology the physical parameters of the layer structure of the package are aligned such, that the measurement and simulation based structure functions overlap each other.

- The structure functions are aligned to each other in an iterative way, starting from the thermal and geometrical parameters of the die, followed by the die attach layer, because the thermal capacitance and thermal resistance values obtained from the structure functions can be directly applied here. Due to the true one-dimensional nature of the heat spreading in this early section, the information provided by the structure functions is most accurate here. Layers located farther from the heat-source, such as different ceramics, or metallic layers have usually well-known parameters, still if they don’t fit, their effective thermal conductivity coefficient should be aligned.

- The calibration process ends when the measurement and simulation based structure functions match over a thermal resistance region which corresponds to the package to be calibrated.

Finding 3.2
Based on the results of the research corresponding to Finding 3. I have shown that the early part of the thermal transient response which is covered by an electrical transient can be regained using thermal simulations. Using the methodology above, based on the thermal part of the measured transient response, the thermal model of the device can be calibrated. The calibrated thermal model’s simulated transient result will inherently contain the early, missing thermal transient section of the measured result. This allows the simulation based electric transient correction of the measured transient response.
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4. Research topic: $R_{\text{thJC}}$ measurement limits of high surface area power semiconductor devices [81]

Research background

There are several ways to define the junction-to-case thermal resistance; however, it is rather challenging to characterize the heat-flow in a package by a single number in an accurate and reproducible way. For many power package families, such as TO-type packages the thermal transient testing and the so-called dual interface method can give reliable results [58].

The diverging point of structure functions from dual thermal transients gives a good picture of the material interfaces in such structures. However, the location and nature of the diverging point strongly depends on the shape and direction of the heat-spreading. If the package area is much larger than the dissipating chip the shape of the heat-flow changes when using different interfaces [29,83]. This causes structure functions corresponding to the two setups deviate much before reaching the case surface. In this research topic the origin of this phenomenon is investigated:

Measurement and simulation results are compared on different large IGBT modules with several modifications in their structure enabling a detailed analysis of the heat-flow path. A comparison is given between heating only a small fraction of a large module and heating all chips.

Problems to be addressed

The junction-to-case thermal resistance is originally defined for devices with nearly perfect one-dimensional heat flow. In such a case it can be defined simply as

$$R_{\text{thJC}} = \frac{\Delta T_{J-C}}{P} = \frac{T_J - T_C}{P}, \quad (4-1)$$

where $T_J$ means the temperature of the junction at a certain powering, $T_C$ the temperature of the case and $P$ the power dissipated at the junction. This quantity is the preeminent figure in product datasheets concerning the steady-state thermal properties.

Considerable deviations from this simple picture are expected when analyzing realistic structures with a three-dimensional heat flow. No single junction temperature can be defined if the temperature changes laterally on the chip [84].

The case temperature may exhibit even larger lateral variation at up-to-date packages which are designed for high power and are usually rather flat. In case of power packages with an external cooling surface which is comparable in area to the size of the chip the picture is mostly clear. These packages are designed to have a mainly 1D heat-flow path towards the cooling surface which makes the diverging point a definite description of the $R_{\text{thJC}}$ value. If the area of the chip (heat source) and the area of the package are not in the same magnitude new challenges arise.
If the chip area is much smaller than the package base itself then the boundary conditions may strongly influence the shape of the heat-spread in the package base [58]. If the package is mounted on the cold-plate using heat-conductive grease the heat spreads in a cone (or pyramid) shape and it does not fill up the whole volume of the heat spreader. However, if the cooling surface is to some extent insulated from the cold-plate, the heat will spread all along the volume of the heat-spread before entering the cold plate.

In other words, the boundary conditions affect the shape of the heat-flow path and also the area of the spreading cone, which is inverse-proportional to the thermal resistance.

Another problem may arise in case of large packages which host more heat sources. Based on the above mentioned phenomena it is not obvious whether for the thermal characterization only one chip or all chips should be turned on [84]. The heat-spread cones starting from each chip may overlap with each-other if the chips are closer than the diameter of the cones. If the heat-sources are close and the cones overlap the heat-flow can be regarded as an essentially 1D flow through the baseplate.

All these problems indicate that a single boundary-condition independent thermal resistance value cannot accurately describe the thermal properties of packages equipped with a large area heat-spread.

**Experimental approach**

In order to quantify the known fact that at different boundary conditions the geometry of the heat-flow in the structure may also be different, Mr.Gao Shan and his team in Samsung designed and manufactured various IGBT module samples with large package surface area (140mm x 70mm). I use these modules as an example to investigate the above mentioned problems.

**Structure**

The general structure of the packages is the same in all cases, shown in Figure 4-1.

All samples host 12 IGBT devices with chip pairs in serial connection. Each of the six serial pairs has distinct electric connections for easier thermal analysis. Two main powering patterns were investigated in this research; thermal transient measurements driving all IGBT-s together (below treated as M setup) and also driving one serial device pair in the middle as highlighted in Figure 4-1 (S setup).
For easier interpretation of the results thermal transient measurements were carried out on different samples. The thickness of the aluminum heat-spreader, the thickness of the copper layer and the area of the die-attach layer below the chips were varied. Although due to confidentiality reasons the real dimensions of the package cannot be disclosed, the relation between the different cases gives enough information for an accurate comparison. The samples and the ratios between the cases are summarized in Table 4-1.

**Table 4-1: IGBT samples used for comparison**

<table>
<thead>
<tr>
<th>Sample Id.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>Standard module, reference to all others</td>
</tr>
<tr>
<td>S2</td>
<td>Module with half copper thickness</td>
</tr>
<tr>
<td>S3</td>
<td>Module with 75% aluminum thickness</td>
</tr>
<tr>
<td>S4</td>
<td>Combination of S2 and S3 cases</td>
</tr>
</tbody>
</table>

**Electric setup**

The thermal response of the IGBT modules was measured with the T3Ster thermal transient tester equipment and its 50A power driving accessory. For the electrical excitation the “MOS-diode” setup was used, where the gate and the collector of each IGBT is interconnected [49]. This circuit behaves as a two-pole device with approximately quadratic characteristics and with a “forward voltage” slightly above the threshold voltage.
For the measurement of the cooling curves the device current was switched from 8A heating current to 500mA sensor current suddenly. The serial pair in the middle yielded a voltage slightly below 7 V at the heating current resulting in 55 W power step (referred as ‘single drive’, S setup below). All 12 devices in series showed approximately 40 V corresponding to 320 W power step (‘multi-drive’, M setup below).

The temperature sensitive forward voltage was calibrated for each device separately at the 500mA sensor current value.

**Boundary conditions**

Due to the large surface area and careful design the junction-to-case thermal resistance of such samples is expected to be very low, which is a must as such modules should be able to bear loads in the kW magnitude range. This makes the selection of the boundary conditions rather challenging. For the realization of the dual interface methodology mostly a ceramic or mylar sheet is used [58]. These work perfectly with smaller power packages or high-power LED-s which have a chip of a few mm² inside and have $R_{thJC}$ values in the 1-5 K/W range.

In case of modern, large surface area packages the selection of the material for changing the package/case interface is a challenge. If the chip size is very small compared to the package surface the inserted layer causes no noticeable change in the transients and the, structure functions. If the chips cover large area of the module and the power level is high the use of such materials may add a huge additional thermal resistance to the system and the junction temperature cannot be kept below the maximum allowed value.

A possible good solution to avoid overheating the devices in the worse boundary condition and still produce significant change in the thermal descriptive functions is to use dry (no thermal grease) or wet surface (thermal grease is used) during the measurements. All packages in this study were measured on a temperature stabilized cold-plate with or without a thermal interface material which was generic silicon grease. The values to be measured were well below 1 K/W so the influence of the thickness of the TIM at the applied pressure was in the same magnitude as the $R_{thJC}$ of the package itself. In order to get comparable and well repeatable results all samples were pushed against the cold-plate by a pneumatic fixture (see Figure 4-3) with 300 kPa constant pressure.
As it is suggested by the theory all measurements were done between two steady-states which meant 120 second pre-heating and 120 second measurement time in practice.

The resulting temperature transient curves for the S1 reference sample are shown in Figure 4-4. In this chart and in all other ones below the curves are denoted as:

SampleID_driven unit_boundary condition, meaning:

SampleID - as shown in Table 4-1

Driven unit - M for multi drive, S for single drive

Boundary condition - G or NG,

where G indicates that a silicon paste TIM was applied between the surface of the package and the cold-plate; NG means that the package was directly mounted on the cold-plate (with a thin air-gap below the package surface).

Both functions run together until app. 0.3 seconds as the main trajectory of the heat flow goes through the same structure. After this point you can see a fast rise in the temperature for the NG boundary where the air gap represents an important obstacle in the heat-flow. Using the NID method, these transient responses can be easily turned into structure functions, which describe the heat-flow path in terms of thermal resistances and corresponding thermal capacitances [25,26]. The cumulative structure function gives information on the volume of the material in which the heat spreads, while its other view, the differential structure function is proportional to the area of the spreading cone.
In the following section the structure functions of the samples listed in Table 4-1 are compared to each other to highlight the nature of the heat-flow in the test package.

**Comparison of the test samples**

In order to take a look inside the reference device the thermal transient response of the module with all chips driven was turned into its cumulative structure function, see Figure 4-5. The layer structure shown in Figure 4-1 is represented well in the corresponding structure function. Arrow number 1 shows the end of the chip, 2 the die-attach layer, the steep section between 2 and 3 shows the spreading in the copper layer, the flat section between 3 and 4 is the thin but poorly conducting insulator layer. From point 4 the spreading in the aluminum layer is visible. Points 5, 6 and 7 are determined by calculating the volume of the aluminum. Point 5 is corresponding to the smallest, block shaped volume in which the heat can spread, simply calculated by the product of the total area of the 12 chips and the width of the aluminum layer. This is surely an underestimation as the heat is expected to follow a conical spreading geometry. Point 7 is selected based on the total volume of the aluminum heat spreader. If you compare it with simulation results, it turns out to be an
overestimation as not the total volume of the aluminum is filled up with heat when the functions start to diverge, see Figure 4-6.

The actual cooling capability is in between the Rth values defined by point 5 and 7. References [85] and [86] suggest an inflexion point approach to find an average Rth corresponding to an effective cooling capability. Now point 6 shows the simple numerical average between the two extreme volumes.

To get the junction-to-case thermal resistance value of the package, the differential structure functions corresponding to the cases with and without grease were compared, see Figure 4-7.

As the figure shows the functions start to diverge at around 0.03 K/W, then run closely parallel before they significantly start to increase their difference. This value is very close to the thermal resistance value where the heat fills up the minimum aluminum volume as mentioned before. The third bar shows 0.126 K/W which corresponds to the total volume of the heat-spreader in Figure 4-5.

The R\(\text{th}_{\text{JC}}\) value to be found should be between these two numbers. An inflexion point can be seen at around 0.08 K/W where the structure function changes its direction. One can assume that this is the point where the temperature distribution of the bottom plate develops [85,86]. The close parallel running of the structure functions from 0.03 to 0.05 K/W are caused by the difference in the area of the heat-spreading cone caused by the different boundary conditions.
The variation of the area of the heat-spreading cone with the resistance of the interface layer used is well proven in the simulation of the single drive case at two boundary conditions, single and double mylar sheet beneath the spreader (Figure 4-8).

![Figure 4-8: Steady temperature distribution at the bottom of the package, (a) thin insulator, (b) thick insulator towards a cold plate](image)

The difference between the hottest point and the coldest in case (a) is around 10 °C while in case (b) it is 15 °C. The distributions clearly show that the geometry of the heat-flow in the package is dependent on the boundary conditions.

To investigate the phenomenon on other package types as well, a half-bridge IGBT power module was tested in the same dual-interface conditions, with grease (G) and without grease (NG) between its cooling surface and the cold-plate. A picture of the power module and the heater/sensor chip inside can be seen in Figure 4-11. The baseplate size of the module was 6.2 cm x 10.7 cm, while the tested chip size was 1 cm x 1 cm.

![Figure 4-9: A half-bridge IGBT power module (left side) and the tested component inside (right side)](image)

The test results corresponding to the G and NG conditions can be seen in Figure 4-10. below, both in cumulative and differential structure function views.
The $R_{\text{thJC}}$ value of the sample is app. 0.26 K/W as indicated in the image, however similarly to the image shown in Figure 4-7, a clear early separation region can be observed starting at app. 0.15 K/W.

In the following section I will get back to the original sample, and demonstrate how the structural changes affect the resulting structural model of the heat-flow path.

**Comparison of single and multi-chip driving**

The IGBT modules used in this study are multi-heat source packages, which means that the thermal resistance will be different when only some chips are driven compared to the fully driven mode. A single device pair in the middle yielded the structure functions of Figure 4-11. The figure also gives some information on the $R_{\text{thJC}}$ of the fully driven package by re-scaling it to the total heating area, supposing it is direct proportional to the number of the heat sources, 6 in our case. This calculation is only an estimation as in the S drive mode there is less interaction between the chips.

The heat-spreader is more effective when driving a few devices, lower thermal resistance value can be expected.

Using the inflexion point for identifying the junction-to-case thermal resistance $R_{\text{thJC,s}}=0.36$ K/W was measured in single drive mode, see Figure 4-11.

If it is re-scaled by the number of the devices driven, $R_{\text{thJC,M}}=0.06$ K/W will be the result for the total module. Compared to the previously measured 0.083 K/W this is really an underestimation proving that the heat-spreading cones overlap with each-other in the multiple geometry. This phenomenon also results in higher temperatures in the sample, which may also trigger some non-linear effects [87]. The $1:n$ scaling, where $n$ is the number of the heat sources would only be valid if
the system could be considered linear; in other words neither the material properties, nor the boundary conditions are temperature dependent. In realistic systems both conditions are met approximately, however the silicone’s specific heat and bulk thermal conductivity coefficient is strongly temperature dependent [88].

\[ R_{th} = \frac{C_v a_s}{c_v} \]  \hspace{1cm} (4-2)

where \( c_v \) is the volumetric specific heat of the material.

Figure 4-12 shows that the chip, die-attach and the beginning of the copper parts of S1 and S2 samples perfectly fit each other in both the S and the M driving modes.
New methods for the investigation of modern packaging materials using thermal transient testing

It is a good proof that the measurements and the calculations give consistent and repeatable results. As the volume of the copper in the S1 sample is twice as high as in the S2 sample, the two curves diverge and S1 reaches a higher thermal capacitance before it turns to the insulator layer.

Although the curvature is not extremely sharp and the values can be read only with some accuracy the figure shows that the curves quickly flatten at specific volumes (indicated by small horizontal lines and numbers meaning mm$^3$ of copper) calculated from the device geometry. In case of S-driven units the flattening starts a bit above 20 mm$^3$ copper for S2 and at 40 mm$^3$ for S1. The turn in the structure functions occurs at 6 times higher copper volume in M-drive mode.

Another important message of Figure 4-5 and Figure 4-12 is that the steep slope of the copper layer has only a very small share in the total thermal resistance. Figure 4-12 also shows that in sample S2 an unknown effect caused poor conduction in the upper insulator layer (or at the joining of the insulator layer to the copper and aluminum), otherwise the structures below the upper insulator are very much the same.

The structure function methodology can point out also small differences. Fitting the cumulative structure functions describing the heat-flow in the S1 and S2 samples after the insulator region in Figure 4-13 we see very good match.
Results with different aluminum thickness

As summarized in Table 4-1 the thickness of the base-plate of sample S3 is 75% of the thickness of sample S1.

Based on the corresponding structure functions the variation in the aluminum thickness does not affect the heat flow path significantly. After the insulator layer the structure functions show similar shape but the actual values differ in the 0.018 K/W to 0.035 K/W interval; then the curves cross and the difference remains stable. On the long run the expected behavior can be observed; the heat spreading in S1 indeed fills up a higher aluminum volume than in S3. From 0.04 K/W we see a very long section where the curves run at approximately 80% ratio, near to the real physical value.

Summary

The dual interface method is a fast and reproducible way to measure the junction-to-case thermal resistance of discrete semiconductor packages. If the area of the chip and the area of the package are similar the heat flow from the junction to the package base is mainly vertical. Although the cumulative structure function shows slightly higher thermal resistance at the same volume when worse cooling is applied at the package base; this difference is small and the separation point of the two curves is unambiguous.
If however the area of the heat-spreader is much larger than the area of the chip then some part of the heat flow will become lateral, the spreading occurs in wide cones varying their sizes also farther from the package surface where the actual boundary is applied. This will result in parallel running structure functions before the “real” separation points.

Measurements carried out on IGBT modules with large surface area and known geometry pointed out that the first section of the heat-flow path is mostly vertical, then the conical spreading dominates. In modules containing many devices the spreading resembles the vertical case again if the spreading cones overlap. Poor heat conductance towards the cooling mount causes lateral spreading in the base.

The volume of the materials in the direction of the vertical heat-flow was well identified with the help of the cumulative structure functions. In case of conical spreading we get an estimated volume of the cone but the values were verified only by introducing a lower and upper limit.

A comparison was given between driving one device set only in the module and driving all of them at the same time. As the first section of the heat-flow path was vertical in both cases, the measured volume of various materials such as silicon and copper was proportional to the number of the driven chips.

In the package base, however, the 3-dimensional heat-spreading and the overlap of the spreading cones causes a systematic difference, the cooling is always better when driving less chips because the heat-spreader is more effective.

**Corresponding research projects**

This work was partially supported by the JEMSiP_3D Joint Undertaking Project of the EU.
Finding 4.
I have experimentally demonstrated that the transient dual interface methodology provides inaccurate results. The reason of the inaccuracy is the change of the heat spreading geometry in the same package at the different boundary conditions.

Finding 4.1
I have demonstrated with experiments and simulations that in case of those power packages, where the cooling area is significantly larger than the heated area of the semiconductor itself, the geometry of the heat-spreading changes already inside the heat spreader, when the dual interface method is applied. The change in the heat spreading geometry causes an early separation point of the structure functions. After the separation point the structure functions run parallel to each other, until the main heat trajectory reaches the real package boundary where the two curves start to diverge significantly. Identifying the first point of separation as the $R_{thJC}$ value leads to an underestimation of the thermal resistance, therefore the second separation point has to be used after the parallel section.

Finding 4.2
I have experimentally demonstrated that in case of multi-heat source packages the ratio of the $R_{thJC}$ value measured from one heat source and the $R_{thJC}$ value measured from n heat sources powered together is not the expected 1:n value. The 1:n assumption is an underestimation of the real thermal resistance due to the overlapping of the heat-spreading cones.
References for research topic 4.


Industrial application of the research results

My research topics although mostly carried out in the framework of EU supported research projects at BME, are also closely related to my work at Mentor Graphics Ltd., therefore each of my findings are somehow related to industrial needs, and some of them even inspired actual product development.

My first research topic, which covers an accurate and reproducible test method for the thermal conductivity coefficient measurement of TIM materials was used as the base idea for the DynTIM, thermal conductivity measurement instrument, which is still part of Mentor Graphics’ product portfolio. By today more than 30 companies use the system on a daily basis for their product development.

The findings of the second, third and fourth research topics serve as references for Mentor Graphics customers today, in order to allow them to do better material selection or to refine their thermal models, or to perform more sophisticated R\textsubscript{thJC} measurements. The model refinement inspired our software team to elaborate a method capable of running several test scenarios automatically, allowing the user to find the optimal simulation parameters more easily. As of today about 80% of our customer base in Japan has adopted this method.
Publications not directly related to research topics covered in this thesis


10. **Andras Vass-Varnai**, John Parry, Gergely Toth, Sandor Ress, Gabor Farkas, Andras Poppe, Marta Rencz,
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In: Proceedings of 14th Electronics Packaging Technology Conference (EPTC'12).
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11. B Plesz, Gy Horváth, **A Vass-Várnai**, 
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12. Székely Vladimír, Kollár Ernő, Somlay Gergely, Szabó Péter Gábor, Juhász László, Renz Márt, Vass-Várnai András,
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13. András Poppe, **Andras Vass-Varnai**, Gábor Farkas, Marta Rencz
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In: Proceedings of the 10th Electronics Packaging Technology Conference (EPTC'08).
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14. L Juhász, A Vass-Várnai, C Dominkovics, V Timár-Horváth:
"Porous Al2O3 Layers for Capacitive RH Sensors”


16. Veronika Timár-Horváth, László Juhász, **András Vass-Várnai**, Gergely Perlaky,
"Usage of Porous Al2O3 Layers for RH Sensing”

17. Veronika Timár-Horváth, László Juhász, **András Vass-Várnai**, Gergely Perlaky,
"Usage of Porous Al2O3 Layers for RH Sensing”