Parallel DC/DC Converters with Multi-Agent Based Multi-Objective Optimization for Consumer Electronics

Peter Bartal, János Hamar and István Nagy
Budapest University of Technology and Economics
Department of Automation and Applied Informatics
Magyar tudósok körútja 2, Q épület
1117 Budapest, Hungary
Email: {bartal, hamar, nagy}@get.bme.hu

***Abstract*—Consumer electronic devices have become a part of our everyday lives. A statistically non-negligible percentage of electric loads on the power network is represented by these devices. Consumer electronics notoriously consume DC power, at several voltage levels ranging anywhere from 1.8 to 24 V, in the absence of unified standards. As a consequence, each load is served from the AC network through several conversion stages, which is not the most efficient solution. The problem of efficiency exists not only on a global level, but locally, too. On a local level efficiency can be improved by connecting several converters in parallel and setting their operating point as close to the maximum efficiency point as possible. This can be implemented by means of multi-agent based load sharing algorithms [1]. These intelligent agents (IA) are negotiating at the load distribution between converters and aim at achieving maximum overall efficiency. Other optima can also be targeted at the same time. The paper presents a model based on DC/DC buck converters and its experimental verification.**

I. Introduction

In recent years consumer electronics have won over tremendous number of users, the electronic gadgets sold in the last few years can be counted by hundreds of millions. They include personal computers, tablets, mobile phones, CD/DVD players, MP3 players, printers, digital cameras, electric toothbrushes, electric razors, etc. Despite the very wide variety, all these devices have one thing in common: they all work with DC power and therefore need a power conversion to feed them from the 120/230 AC network operating at 50/60 Hz. This network has been designed at a time, when most loads were fixed speed drives or lighting installations. The rectification of the AC voltage for today's consumer electronic appliances is done locally, for each device separately, whereas it would be more efficient to have a DC power distribution network that intelligently recognises the load and sets the output voltage for each socket, according to the needs of the connected device.

With the recent worldwide push for "green" technologies and innovations and the impossibility to curb the steady increase in energy consumption, other solutions are needed. In this paper a solution is proposed to make the AC/DC conversion chain more efficient. First a rectifier will produce a "base" DC voltage V_{in} feeding the DC/DC converters connected in parallel. They provide jointly the necessary power for the load, while insuring maximum efficiency at all times. This is possible due to the intelligent agent based digital control implemented into the microcontroller driving the converters. The decisions leading to optimal operation will be taken by the agents (able to communicate with each other and the load) through negotiations. Furthermore, the converters will be able to gather information on the load they serve. This will make it possible to determine the voltage level required by the load, adjusting the operation of the converter(s).

II. Intelligent Agent Based Control

The research described in this paper aims towards implementing a working model for the intelligent agent (IA) control of DC/DC converters operating in parallel. The agent based control is independent of the actual converter topology and control, allowing the choice of a simple and widespread converter for demonstration. Along this line, the buck converter was chosen.

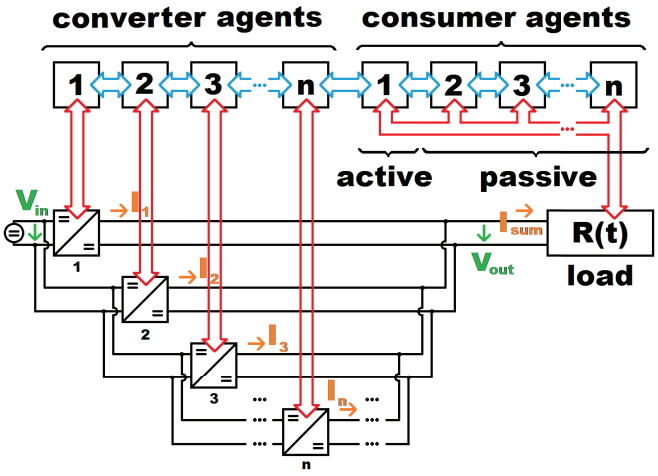

Fig. 1. Proposed system of IA controlled parallel DC/DC converters

Fig. 1 shows the system in a simplified manner. The agents, both converter and consumer agents (IA) are software that is

running on the microcontrollers responsible for the operation of the converters. There are two types of agents: consumer agents and converter agents. Consumer agents are typically assigned to loads, while converter agents are assigned to converters. These two types always work in pairs, meaning that there is a converter agent and a consumer agent for each converter. On start-up a simple hierarchy is established between the agents: an "active" agent is elected, the rest being "passive". While the active agent is working throughout the whole period, when a load is connected, this is not necessarily the case for a passive agent, it depends mainly on the change in the load. The agents have a rank, starting with the active agent, then the passive agents are each assigned a lower rank. This is necessary only to establish a sequence, in which the converters operating in parallel will be turned on or off [2].

In the event of a malfunction, and if sufficient redundancy is built in, the affected agent can pass its role on, to another agent.

III. Optimization

The data for the exemplar buck converter chosen for this project are listed below:

TABLE I
DESIGN PARAMETERS OF THE DC/DC CONVERTERS

Parameter	Symbol	Value
Inductance	L	39 μH
Capacitance	C	680 μF
Parasitic resistance of the inductor	R_L	20 mΩ
Parasitic resistance of the capacitor	R_C	20 mΩ
Forward voltage of the diode	V_f	1.3 V
On-state resistance of the switch	R_{on_S}	0.065 Ω

The agents are able to improve the operation of the overall system, based on optimization criteria that have previously been established. The system can accommodate several, even conflicting optimization criteria, e.g. maximum energy efficiency and minimum output voltage ripple. In such cases the system will prioritize these criteria, depending on the weight each has previously been assigned. Theoretically as many such criteria can be defined as desired.

Each control agent has a cost function it tries to minimize. This cost function establishes the target the agent has to achieve. By weighting the individual targets, multi-objective optimization can be achieved.

Let c_{η_i} be the cost function for efficiency of the i^{th} control agent:

$$c_{\eta_i} = 1 - \eta\left(I_{L_i}\right) \tag{1}$$

where I_{L_i} is the inductor current of the i^{th} converter and η is the efficiency as a function of this current. A reasonable approximation is to assume $I_{L_i} \approx I_{out_i}$ and therefore it is safe to assume that the efficiency curves plotted as a function of I_{out} are almost the same if plotted as function of I_L. Thus, it is true that $c_{\eta_i} = 1 - \eta\left(I_{L_i}\right) \approx 1 - \eta\left(I_{out_i}\right)$.

The efficiency curve of a buck converter has a maximum for a given current. If the agent "knows" the value of this current, it will try to set the operation point of its converter as close to it as possible.

The efficiency curve for the buck converter is pictured below (Fig. 2), based on experimental data. Clearly, the critical working region is under light load, where small changes in the load current lead to large variations in efficiency. Accordingly, it is not justifiable economically to have a large converter working at partial load.

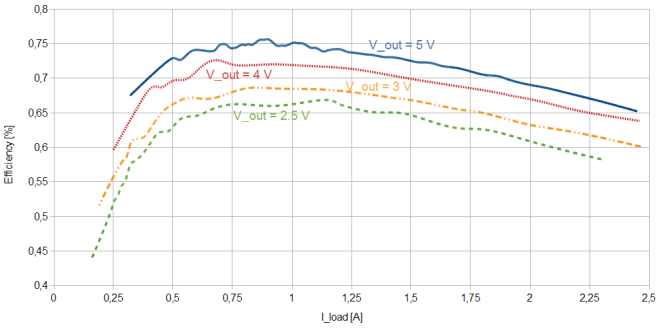

Fig. 2. Measured efficiency curves of the buck converter

The curve has a peak at a given load current. The optimum current, for which the efficiency attains its maximum, can be determined from the expression for the efficiency curve:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \tag{2}$$

where P_{out} and P_{in} are the output and the input power of the converter and P_{loss} represents the losses of the converter:

$$P_{loss} = P_{switch} + P_f + P_{on} + P_L + P_C \tag{3}$$

with losses due to switching (P_{switch}), forward voltage of the semiconductor devices (P_f), on-state losses (P_{on}) and the losses in the inductor (P_L) and the capacitor (P_C) [3], [4].

The peak of the efficiency curve for a given output voltage is to be found where:

$$\frac{\partial \eta}{\partial I_{out}} = 0 \tag{4}$$

and the solution is (see appendix):

$$I_{opt} \simeq \sqrt{\frac{f_s C_s V_{in}^2}{R_{on_S} D^3 + R_{on_D}(1-D) + R_L}} \tag{5}$$

with f_s the switching frequency, C_s the parasitic capacitance of the controlled switch, R_{on_S}, R_{on_D} the on-state resistances of the controlled switch and the diode, respectively, and D the duty ratio. The duty ratio can be approximated with $D \approx V_{out}/V_{in}$. This approximation is more accurate at higher efficiencies.

Another cost function is defined, $c_{\Delta u_i}$, the minimization of the output voltage ripple by increasing f_s. It will clearly be in conflict with the maximum efficiency criterion defined in (1), since higher switching frequencies lead to higher losses. The total cost function that needs to be minimized is then:

$$c_{total} = \min_{I_{out_i}, f_s} \left\{ w_1 \sum_{i=1}^{n} c_{\eta_i} + w_2 \sum_{i=1}^{n} c_{\Delta u_i} \right\} \quad (6)$$

where w_1 and w_2 are weighting factors. Based on these, the agents will negotiate a lower efficiency, but also lower output voltage ripple or the opposite. The weighting factors can be selected to best suit the needs of a given application and may be selected by the consumer itself. In more advanced applications it is possible to use functions instead of the factors.

If identical DC/DC converters are connected in parallel, it also implies that the efficiency curves of the converters are the same. To maximize the utility function under light load, a possible solution for load current distribution can be that $m-1$ DC/DC converters out of n (with $m \leq n$) operate in their optimal point (with maximum efficiency), that is with the associated current I_{opt}, while the m^{th} converter provides the remaining current, resulting in a total current of: $I_{sum} = (m-1)I_{opt} + I_m$, required by the consumer.

In practical settings the efficiency of the converter is difficult to calculate. Therefore, assuming as earlier that $I_{L_i} \approx I_{out_i}$, the cost function for efficiency has been redefined. The cost of lower efficiency is proportional to the distance of the working point from the optimal point of operation and also proportional with the current ripple, which causes additional losses:

$$c_{\eta_i} = \begin{cases} (I_{opt} - I_{L_i})\,\Delta I_{L_i}, & I_{L_i} < I_{opt} \\ 0, & I_{opt} \leq I_{L_i} < I_{max} \end{cases} \quad (7)$$

where ΔI_{L_i} is the inductor current ripple of the i^{th} converter.

The cost function for the output voltage ripple is:

$$c_{\Delta u_i} = \Delta I_{L_i} \quad (8)$$

The motivations behind using such simple expression for $c_{\Delta u_i}$ are both the fact that the ripple in the inductor current is proportional to the output voltage ripple and the need to obtain efficient code.

Replacing (7) and (8) in (6) yields as total cost function for minimization:

$$c_{total} = \begin{cases} \Delta I_{L_i}\left(w_1\left(I_{opt} - I_{L_i}\right) + w_2\right), & I_{L_i} < I_{opt} \\ w_2 \Delta I_{L_i}, & I_{opt} \leq I_{L_i} < I_{max} \end{cases} \quad (9)$$

To calculate the total efficiency of the converters in parallel, the following formula was used, assuming $\eta_1 = \eta_2 = \ldots = = \eta_{m-1} \neq \eta_m$ (the m^{th} converter works with a different current than I_{opt}, while all other converters work at the same — maximum — efficiency):

$$\eta = \frac{\sum_{i=1}^{m} P_{out_i}}{\sum_{i=1}^{m} P_{in_i}} = \frac{\sum_{i=1}^{m-1} (\eta_i P_{in_i}) + \eta_m P_{in_m}}{\sum_{i=1}^{m-1} P_{in_i} + P_{in_m}} \quad (10)$$

In the region of light load, with load currents below I_{opt}, the equal load sharing strategy yields weaker results in terms of efficiency than having $m-1$ converters (out of the m required by the load) working at maximum efficiency and one contributing the missing amount, as the IAs would decide. This is illustrated by the results in Table II. The table shows that the difference in efficiency grows larger as the load becomes lighter.

TABLE II
EFFICIENCY OF THE DC/DC CONVERTERS FOR VARIOUS LOADS

R_{load} [Ω]	5	10	15	20	25
η_{eq} [%]	73.86	72.91	72.18	71.17	69.94
η_{IA} [%]	75.77	78.03	75.77	78.03	80.29
$\Delta\eta$ [%]	0.45	5.12	3.58	6.86	10.34

The efficiencies are given as a function of the load resistance, η_{eq} is the efficiency in the case of equal current sharing and η_{IA} is the efficiency in the case of IA control. The difference is displayed on the last row of the table.

IV. SIMULATIONS AND TEST RESULTS

A model of the four converters has been built in Matlab/Simulink. Simulations for various loads have been carried out, from which the 1 Ω load connected to an output voltage of 5 V and the 3 Ω load connected to the same voltage are presented in Fig. 3. It can be seen that the converters successively go on-line, as the agents find it necessary to turn on more and more converters, until finally the load is properly served. The optimum current has been set to 1.5 A in the simulations. The figures show that the converters will distribute the load according to the strategy described above, with $m-1$ out of the necessary m converters supplying I_{opt} and the m^{th} converter the rest. In the case of a lighter load (3 Ω), only two converters suffice. Again, one of them is working at optimum efficiency and the remainder comes from the other converter.

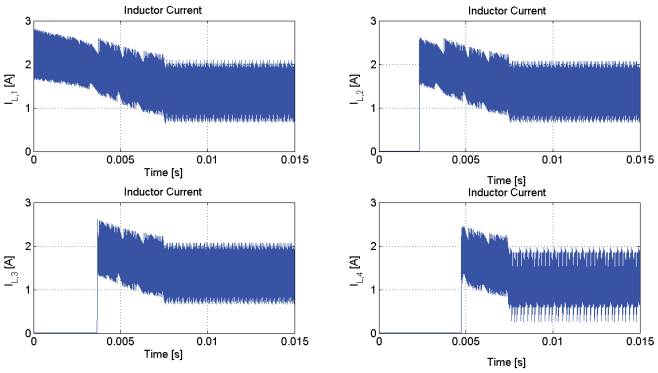

Fig. 3. Simulated inductor currents for output voltage $V_{out} = 5$ V and load of 1 Ω

The test setup is shown in Fig. 5. DC/DC buck converters of the type PICDEM SMPS from Microchip were used, which come in pairs on a breadboard and are controlled by a dsPIC30F2020 microcontroller. In the present example four converters were connected in parallel. Their parameters have already been listed in Table I.

Throughout the tests the converters were working with sliding mode control (SMC) [5], [6]. The optimum current

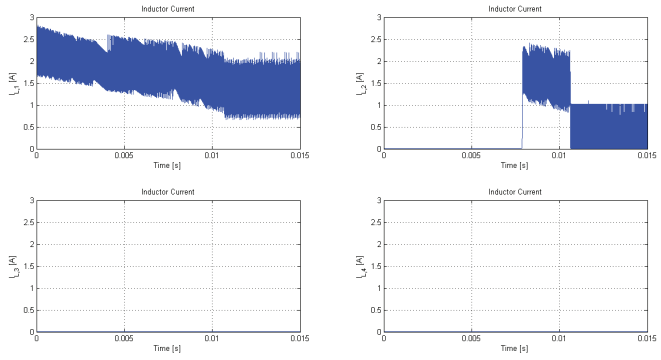

Fig. 4. Simulated inductor currents for output voltage $V_{out} = 5$ V and load of 3 Ω

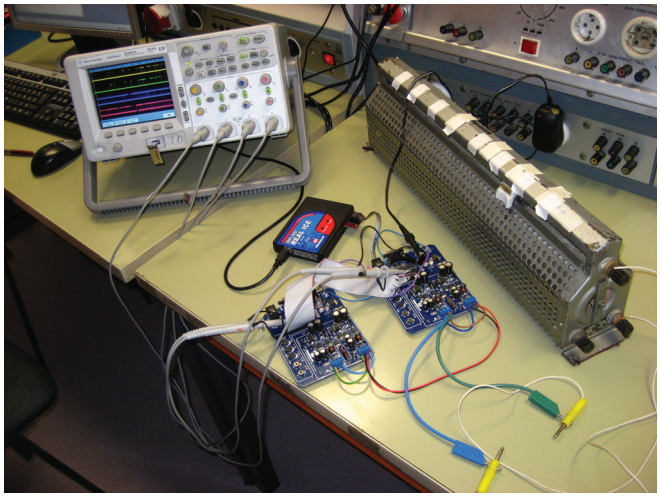

Fig. 5. Experimental setup

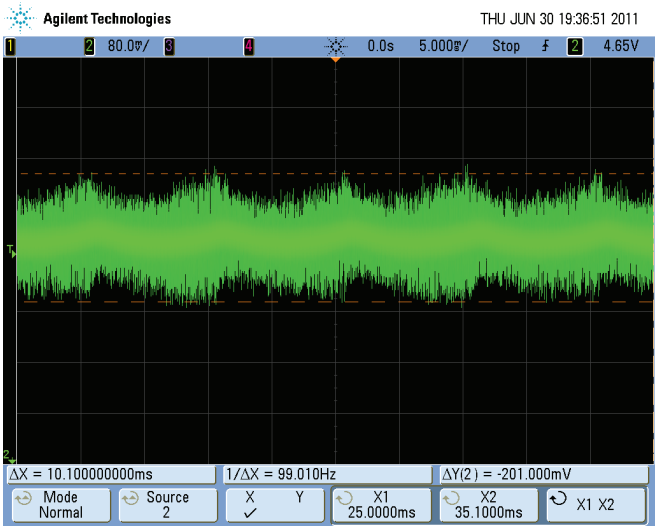

Fig. 6. Peak-to-peak output voltage ripple (ΔV_{out}) for $w_1 = 10$, $w_2 = 1$ ($V_{out} = 5$ V, $R_{load} = 8.5$ Ω) — as measured between the two horizontal dashed lines

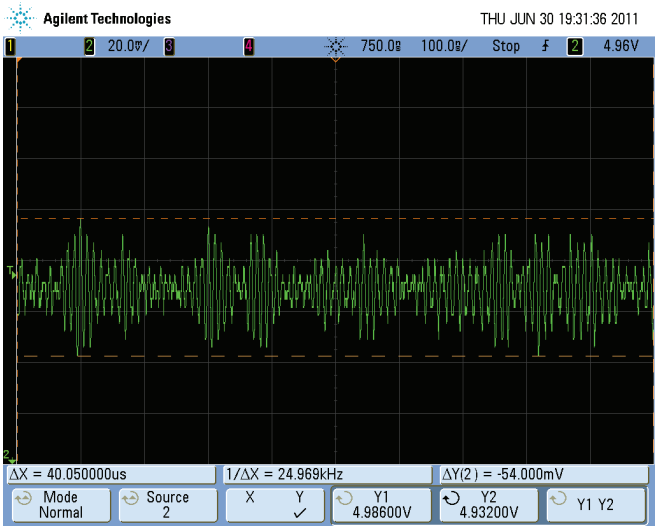

Fig. 7. Peak-to-peak output voltage ripple (ΔV_{out}) for $w_1 = 1$, $w_2 = 10$ ($V_{out} = 5$ V, $R_{load} = 8.5$ Ω) — as measured between the two horizontal dashed lines

was set to $I_{opt} = 0.5$ A. (Automatic calculation of the optimum current had not been implemented yet.) The ripple of the sample inductor current is determined by the hysteresis bandwidth set by the IAs. The larger the hysteresis is, the lower the switching frequency, thus improving efficiency. The task of the agents is to find the right compromise in this situation. The output voltage ripple is presented in two situations: when in (6) the weighting factors are $w_1 = 10$, $w_2 = 1$ (Fig. 6) and $w_1 = 1$, $w_2 = 10$ (Fig. 7). In the first case, with more relaxed conditions for the ripple, it was around 200 mV and in the second case, with tighter requirements, the ripple was 54 mV.

The gate signals of the MOSFETs driven by the microcontroller are shown in Fig. 8 and Fig. 9, showing the behaviour of the converters under different loads. Consistently with the simulation results, the appropriate number of converters is turned on or off, depending on the needs of the load.

V. Conclusion

A multi-agent based system with DC/DC converters connected in parallel with multi-objective optimization capabilities has been presented. Both simulations and laboratory tests have been carried out. The multi-agent based multi-objective optimization algorithm presented has achieved to find a compromise between two conflicting optimization criteria, namely maximum efficiency and minimum output voltage ripple, with significant efficiency improvement under light load conditions.

Future work will include the exploration of other approaches for output voltage ripple reduction in conjunction with more advanced negotiation techniques for the IAs. Also, communication delays and other related issues will be analysed.

Appendix

The various losses are defined as [3], [4] follows:

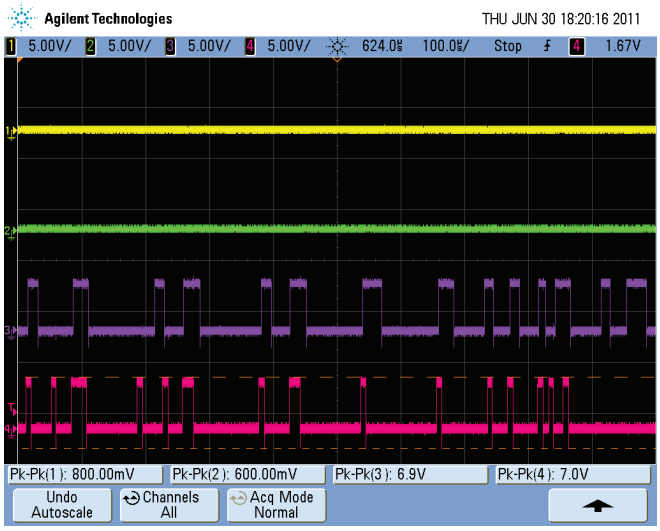

Fig. 8. Gate signals of the MOSFETs in four converters for $V_{out} = 5$ V, $R_{load} = 5.5\ \Omega$

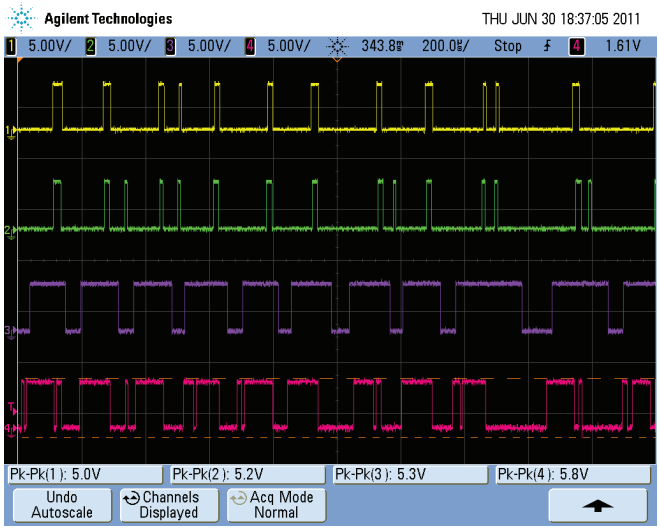

Fig. 9. Gate signals of the MOSFETs in four converters for $V_{out} = 5$ V, $R_{load} = 2\ \Omega$

Switching losses

$$P_{switch} = f_s C_s V_{in}^2 = \frac{f_s C_s R_{load}}{D^2} P_{out} \tag{11}$$

Forward voltage losses in semiconductor devices

$$P_f = (1-D)\, V_{f_D} I_{out} + V_{f_S} I_{out} D \tag{12}$$

On-state losses of the switches

$$P_{on} = V_{on} I_{max} t_{on} f_s \approx R_{on_S} I_{in}^2 D + R_{on_D} I_{out}^2 (1-D) \tag{13}$$

Losses of the inductor

$$P_{R_L} = R_L I_{out}^2 = \frac{R_L}{R_{load}} P_{out} \tag{14}$$

Losses of the capacitor

$$P_C = R_C I_C^2 = \frac{\Delta i_L^2}{12} R_C = \frac{(1-D)^2 R_L R_C}{12 f_s^2 L^2} P_{out} \tag{15}$$

where I_C is the RMS value of the current through the capacitor:

$$I_C = \sqrt{\frac{1}{T}\int_0^T i_C^2 dt} = \frac{\Delta i_L}{\sqrt{12}} \tag{16}$$

Replacing (11) – (15) in (3) makes the calculation of the losses possible. Subsequently the efficiency can be determined from (2). Then, (4) can be rewritten as:

$$\eta = \frac{V_{out} I_{out}}{f_s C_s V_{in}^2 + I_{out}\left[V_{f_S} D^2 + (1-D) V_{f_D} + V_{out}\right]} + \\ + \frac{V_{out} I_{out}}{I_{out}^2\left[R_{on_S} D^3 + R_{on_D}(1-D) + R_L\right]} \tag{17}$$

After derivation the optimum current for the converter can be obtained, using (4).

ACKNOWLEDGMENT

The authors wish to thank the Norwegian Financial Mechanism, the Hungarian Research Fund (OTKA-NNF 78703, TO 72338, OTKA K72338) and the Control Research Group of HAS for their financial support as well as the János Bólyai Research Fellowship of the HAS. This work is connected to the scientific program of the "Development of quality-oriented and cooperative R+D+I strategy and functional model at BME" project. This project is supported by the New Széchenyi Plan (Project ID: TÁMOP-4.2.1/B-09/1/KMR-2010-0002).

REFERENCES

[1] J. Hamar and A. Toth, "Agent-Based Control of Parallel DC-DC Converters", *European Conference on Power Electronics and Applications* (EPE 2009), Barcelona, Spain, September 8-10, 2009

[2] T. D. Sepsi and P. Bartal, "Cascaded Control for DC-DC Buck Converters Using Multi-Agent Systems Approach", *Automation and Applied Computer Science Workshop* (AACS 2010), Budapest 2010, June 25

[3] N. Das, M. Kazimierczuk, "Power Losses and Efficiency of Buck PWM DC-DC Power Converter", *Electrical Insulation Conference and Electrical Manufacturing Expo*, 2005

[4] Z. Leng, Q. Liu, J. Sun, J. Liu, "A research of efficiency characteristic for Buck converter", *2nd International Conference on Industrial Mechatronics and Automation*, ICIMA 2010, Wuhan, China

[5] T. L. Skvarenina, "Power Electronics Handbook", Industrial Electronics Series, 2002

[6] M. Ahmed et al., "Implementing simple procedure for controlling switch mode power supply using sliding mode control as a control technique", *Proc. of XIIIth Intl Symp. on El. App. and Tech.*, SIELA 2003, Plovdive, Bulgaria