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New Methods and Supporting Tools for the Thermal Transient Testing of Packages

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Abstract

A complete toolkit for the accurate dynamic characterization of packages is introduced in the paper. After giving the theoretical background it is shown that convolution and deconvolution methods can directly generate all usual package descriptions in time and frequency domain from a single transient measurement – in such a way significantly reducing package development and evaluation time. A practical example demonstrates the usage of the differential structure function that is an excellent tool for characterizing the package and detecting die-attach and packaging failures – and also useful for correct measurement of thermal conductivity or emissivity parameters. Some hardware devices, i.e. thermal transient tester equipment and thermal test chips that can produce the required accurate, crisp and noise free transient measurements are presented in the last section of the paper.

Introduction

Nowadays, with the always growing power levels in integrated circuits the thermal characterization of packages becomes a most important engineering task. Contemporary tools give a detailed picture of the time-transient and frequency domain behavior of the package and help to detect packaging and die-attach problems.

Heat conduction and convection mechanisms are mostly linear effects, i. e. when increasing power levels the temperature changes grow proportionally. There are some exceptions, e.g. silicon has nonlinear heat conductance at higher temperatures and radiation effects are of higher quotients, still these effects are not very steep in the temperature range used when characterizing packages and so they can be linearized without a significant loss of accuracy.

Thus, methods and results of linear network theory can be successfully used for measuring and simulating packages.

Network theory shows that the time-domain response of a linear circuit on an arbitrary excitation can be calculated if some special descriptive functions of the circuit are known. These are the *w(t)* weight function, the response on the Dirac-d excitation (approximated by a very short pulse of known energy) and the a*(t)* response function on the unit-step excitation. If network elements are known these descriptive functions can be easily calculated and the *T(t)* temperature response of the circuit on different *P(t)* power excitations can be gained using the *convolution integral*:

$$T(t) = \int_0^\infty w(y)\, P(t-y)\, dy \qquad \text{or shortly} \qquad T(t) = w(t) \otimes P(t). \tag{1}$$

From (1) for the descriptive functions $a(t) = \int_0^t w(y) \cdot 1\, dy$, $\qquad w(t) = \dfrac{da(t)}{dt}$ (2)

Time-domain and frequency-domain results are equivalent and can be derived from each other through the Fourier transformation.

While simulation can be carried out in all domains and for any excitation, frequency domain measurements in a wide range are rather tedious and the use of very short pulses of high power is also problematic. Measurements are mostly realized as thermal transient measurements on a system excited by a power step, i.e. the a*(t)* step response function of the package is measured (Figure 1). However, transforming the measured data into thermal resistance, thermal capacitance or conductivity values or further into geometrical dimensions is not a straightforward task.

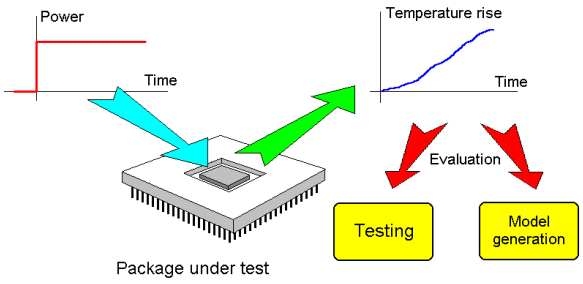

Figure 1 **Thermal transient testing of a package**

A large number of papers deal with the evaluation of the measured heating or cooling curves, since the early paper from Siegal [1], through Szekely, Sofia and Oliveti [2-4]. Paper [2] has shown for the first time a direct transformation method that is capable to deliver even material structural data from the measured thermal transient curves. In paper [5] it is proved that the convolution method can

be used in a reverse way, i.e. network structures can be identified from the transient response (network identification by deconvolution, NID method).

MicReD provides now a comprehensive and coherent set of hardware and support tools (transient tester, thermal test chips, simulators) that constitute a complete toolkit for measuring and simulating package characteristics in time-domain and frequency-domain.

After summarizing the theoretical background (this section can be skipped by those interested in the usage only) the novel tools are presented, followed by some practical examples.

Theoretical background

An infinitesimal part of material can transfer heat to neighboring regions and can store a certain amount of heat, i.e. any small cube in the structure can be represented by an equivalent circuit of Figure 2. Network theory shows that when power is applied on a *single point* of the structure an equivalent one-dimensional circuit can be built up which gives the same temperature response (in other terms, it has the same *driving-point* or *self-impedance*). *Transfer impedances* describe the temperature response at locations farther from the excitation point.

Equivalent circuits can be reduced to less elements still describing the structure with a certain accuracy. Network theory prefers two canonic model networks of a single port system that can be directly synthesized and can be easily transformed into each other, the Foster type (Figure 3 a) and the Cauer type (Figure 3 b) representation.

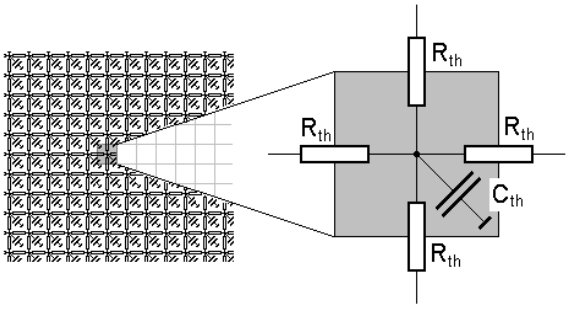

Figure 2 Simple model of a real physical structure

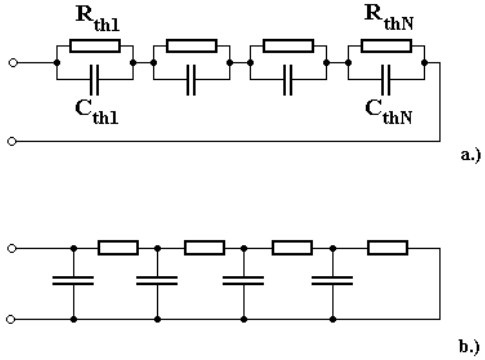

Figure 3 Foster (a.) and Cauer (b.) type representation of physical structures with finite time constants

If we apply a P power step to the simplest model consisting of a single R_{th} and C_{th} element the temperature will rise according to $T(t) = P\,R_{th}\left(1-\exp(-t/t)\right)$, where $t = R_{th}C_{th}$ is the time constant of the system.

A finer approach can be given introducing more time constants, in this case the temperature response is the sum of the appropriate exponential functions, as one can deduce from the equivalent Foster circuit of Figure 3a:

$$T(t) = P\sum_{i=1}^{N} R_{thi}\left(1-\exp(-t/t_i)\right) \qquad (3)$$

Instead of using the transient response like (3) or the equivalent Foster chain of Figure 3a we can characterize a network by giving the position and magnitude of its t_i time constants (Figure 4a) .

Real physical structures are continuous, they can be described by an infinite number of time constants, forming a continuous time constant density function (Figure 4b).

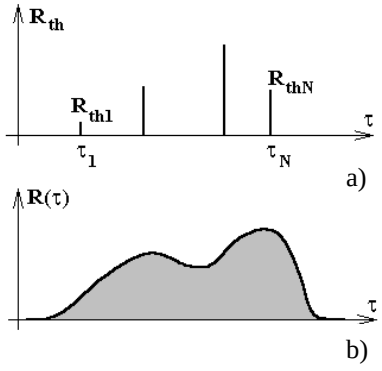

Figure 4 Time constants in a lumped element system (a) and in a distributed parameter system (b)

The new methods

MicReD tools share a set of algorithms for processing transient data from various sources like the *T3Ster*® transient tester, thermal chips or simulators. The backbone of these procedures can be described as follows:

a) Preparatory steps. The first step is filtering electric transients and smoothing the *a(t)* transient curve. For further calculations it is most useful to introduce the $z = \ln(t)$ logarithmic time variable and then to calculate and store the auxiliary *da(z)/dz* derived function.

In Figure 5 a smoothed transient response of a PG144 package is shown, recorded by a TMC81 thermal test chip at three different locations.

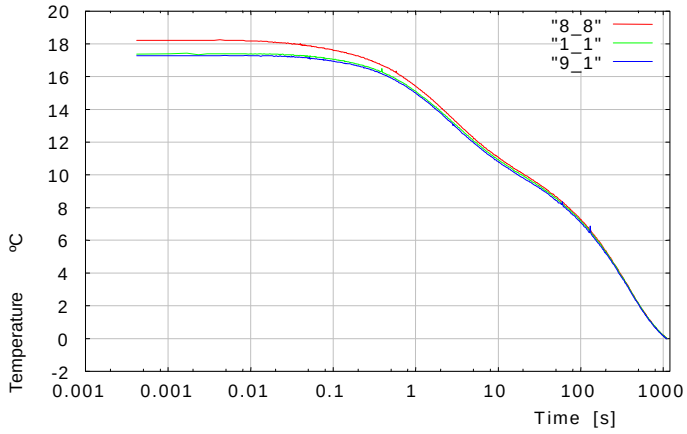

Figure 5 Temperature transient on a CMOS chip in a PGA144 package obtained at different locations

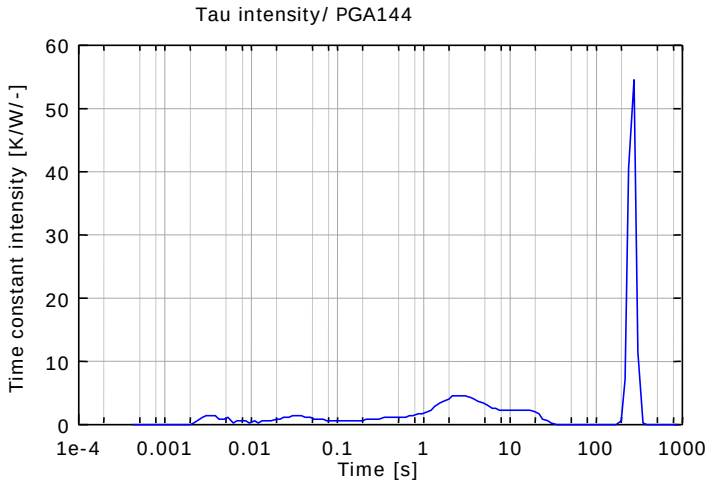

Figure 6 Time constant spectrum calculated from the transient curve at the driving point (8_8) of Figure 5

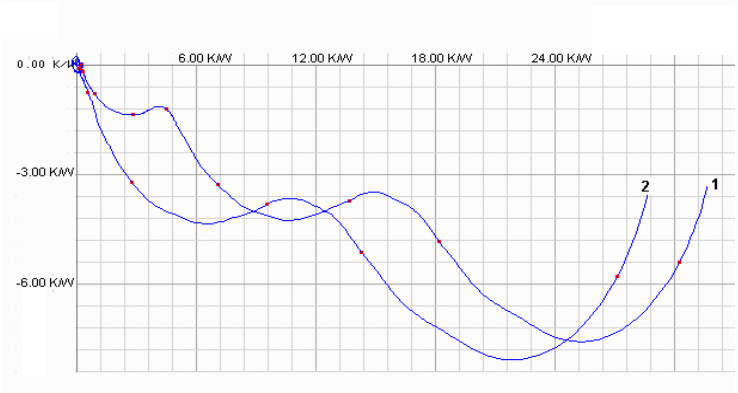

Figure 7 Driving point (1) and transfer (2) thermal impedance of a chip in PGA144 package

b) Calculating time constant spectrum.

Based on (1), (2) and (3) we obtain the following differential equation for the auxiliary derived function:

$$\frac{da}{dz} = R(z) \otimes w(z), \qquad (4)$$

where $w(z) = \exp(z - \exp(z))$.

For the required deconvolution operation the Bayes iteration method is used. Although deriving the time constant spectrum upon (4) is mathematically simple and elegant, only crisp and noise free transient recording and high precision operations give correct results.

c) Calculation of complex loci.

In the very important case of harmonic excitations driving-point and transfer impedances for all frequencies can be displayed on Bode and Nyquist diagrams. These latter ones are also known as complex loci and show the real and imaginary part of the impedance by the frequency as parameter. Figure 7 shows driving-point (1) and transfer (2) impedances, calculated from a *T3Ster*® measurement on a PGA144 package.

In the algorithm of the transformation into the frequency domain we start from the *da(z)/dz* function. A simple and fast convolution algorithm provides the required results [7] :

$$\mathrm{Re}(\boldsymbol{Z}(W)) = \mathrm{W_R}(W) \otimes da/dz|_{\Omega=-z}\,,$$
$$\mathrm{Im}(\boldsymbol{Z}(W)) = \mathrm{W_I}(W) \otimes da/dz|_{\Omega=-z} \qquad (5)$$

where

$$\mathrm{W_R}(W) = \cos e^{\Omega}\,, \quad \mathrm{W_I}(W) = -\sin e^{\Omega}\,.$$

The mathematical difficulties of calculating the functions of (5) and a simple way to overcome the problems are presented in [7].

d) Calculation of the pulse thermal resistance.

The pulse thermal resistance (impedance) diagram characterizes the dynamic thermal features of a package in applications with a periodic pulse excitation (e.g. switching power supplies).

In this diagram the temperature of the device is shown as a function of the period length, parameterized by the duty-cycle factor. The fact that the temperature of the device will be lower due to the periodic heating/cooling when the switching time is short can be seen in Figure 8. For a zero duty-cycle and long switching-on time we get the original heating transient on power step excitation again. Lower temperatures are displayed in this diagram as caused by lower equivalent thermal resistance.

We can directly calculate the R_{thp} functions from the time-constant spectrum with a simple convolution equation [8]:

$$R_{thp}(z = \ln t, d) = R(z) \otimes w_{rthp}(z, d)\,, \quad \text{where} \quad w_{rthp}(z, d) = \frac{1 - \exp(-\exp(z))}{1 - \exp(-\exp(z)/d)} \qquad (6)$$

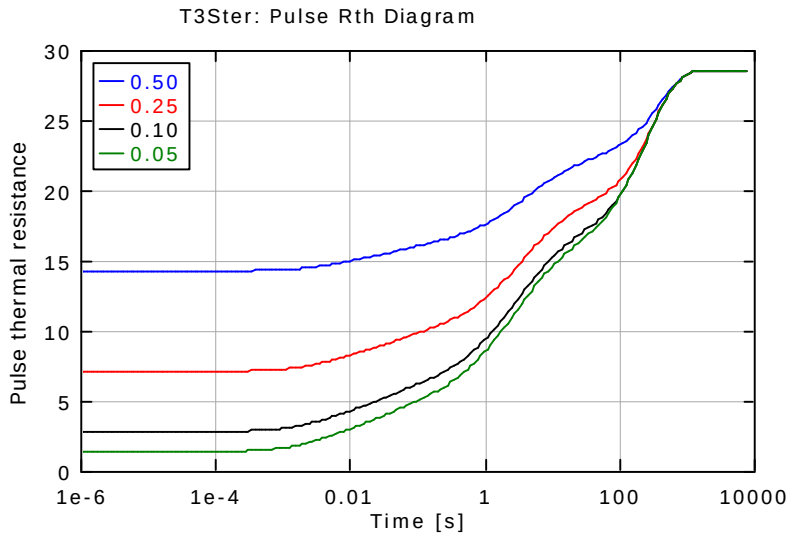

Figure 8 Pulse thermal resistance diagram of a PGA144 package

Figure 8 shows R_{thp} functions calculated from a transient measurement by the *T3Ster*® equipment. The curves are parameterized by the duty factor of a theoretic square-wave dissipation function.

d.Calculation of structure functions

As shown before knowing the time constant density of a system a Foster equivalent circuit may be constructed by approximating the R(τ) function by infinitesimally narrow boxes with the height of R(τ), determining each a parallel RC pair in the Foster chain.

It is useful to transform this network to its Cauer equivalent which can be better interpreted in the physical terms of the heat transport in thermal systems. (As we saw in Figure 2, real thermal capacitances are defined to the ambient only).

From this Cauer type circuit we can draw up the so-called *cumulative structure function* or PROTONOTARIOS-WING function [6], which is the $\mathbf{C}_S$ sum of the thermal capacitances in the function of the $\mathbf{R}_S$ sum of the thermal resistances, measured from the point of excitation towards the ambient (Figure 9).

On this monotonously increasing function the plateaus represent new materials, their widths give the related thermal resistances. The linearly increasing intervals represent fields with heat propagation over linearly increasing areas.

A descendant of the Protonotarios-Wing function is the *differential structure function* introduced in [2]. The differential structure function is defined as the derivative of $\mathbf{C}_S$ the cumulative thermal capacitance with respect to the $\mathbf{R}_S$ cumulative thermal resistance, by

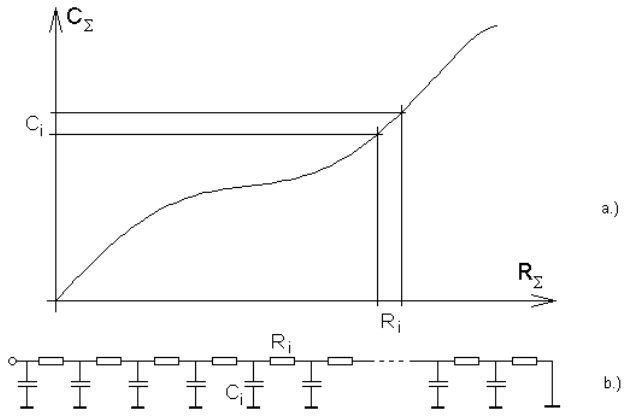

Figure 9 The cumulative structure function and the related Cauer equivalent circuit

$$K(R_\Sigma) = \frac{dC_\Sigma}{dR_\Sigma} \tag{7}$$

This function is referred usually shortly as the *structure function*. Since the capacitance of a *dx* wide slice of a matter (Figure 10) is $dC_\Sigma = cAdx$, and the resistance of this slice is $dR_\Sigma = dx/lA$, where c is the volumetric heat capacitance, l is the thermal conductivity and A is the cross-sectional area of the heat flow, the value of the structure function is

$$K(R_\Sigma) = \frac{cAdx}{dx/lA} = clA^2 \tag{8}$$

This value (sometimes designated with *S*) is proportional to the c and l material parameters, and to the square of the cross sectional area of the heat flow, consequently it is related to the structure of the system.

In other words: this function provides a map of the square of the heat-current flow cross section area as a function of the cumulative resistance.

Measured structure functions of power transistors on a cold plate are presented in Figure 11. In this functions the local peaks usually represent reaching new surfaces (materials) in the heat flow path, and their distance on the horizontal axis gives the partial thermal resistances between these surfaces. If we know the l and c parameters for the used materials, even the cross section area vs. distance map can be constructed for the examined structure [7]. A more detailed explanation of the curves of Figure 11 will be given below in the Examples section.

Obviously, if the heat-flow follows (dominantly) a single path, the derived

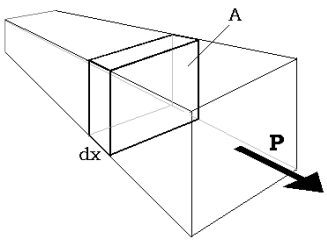

Figure 10 Interpretation of the *structure function*, P is the heat current

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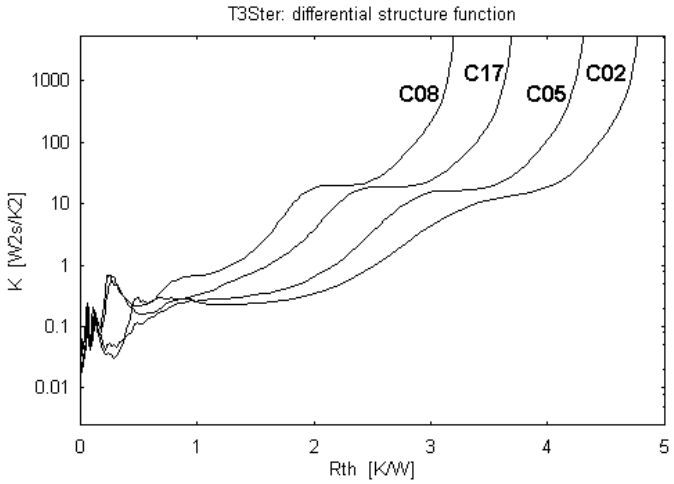

Figure 11 Structure functions of power transistors on a cold plate, measured and evaluated by *T3Ster*® [9]

model corresponds directly to the physical structure, enabling the reconstruction of this structure If, however, there are comparably important paths of the heat flux e.g. towards the top surface, the sides and the pins of the package etc. the physical interpretation of the resistance / capacitance fractions becomes difficult. In case of complex, 3D streaming the derived model has to be considered as an *equivalent* physical structure providing the same static or pulse thermal resistance as the original structure, not as a reconstruction of the physical structure to be modeled.

e) Generating reduced order models

In step d) we generated high order equivalent RC models for enhanced accuracy. As it is pointed out in [10], producing reduced order models is useful for getting results extremely fast in subsequent analyses.

Example

In our example we reveal that the structure functions are extremely useful in the evaluation of the thermal behavior of packages. They can be used to determine partial and interface thermal resistances, and as such, they are good candidates for being used for in-line testing of the die attach quality, or for measuring very small R_{th} values. They can be also used to measure *effective thermal conductivity* values of printed circuit boards, *emissivity* values ([11],[12]), or *? thermal conductivity parameter* of highly conductive materials. Now an example will be presented where determining partial thermal resistances helps examining die attach quality.

Die attach failures frequently can not be detected by standard R_{th} measurements, and even in cases where a time-consuming steady state R_{th} measurement could detect the problem, only transient measurements may be contemplated for in-line testing. The differential structure function offers the possibility of locating the material transitions in the heat flow path, characterized by the cumulative thermal resistance, and finding the partial thermal resistances between the different locations. Comparing the structure function of the measured device with that of a known good device the location and the value of the increased partial thermal resistance may be easily determined.

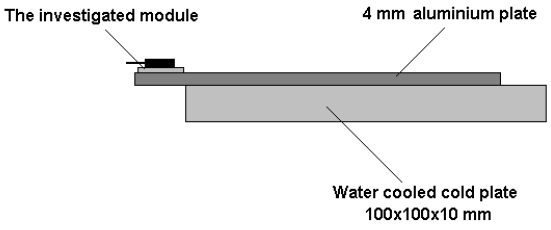

Figure 12 The measurement arrangement

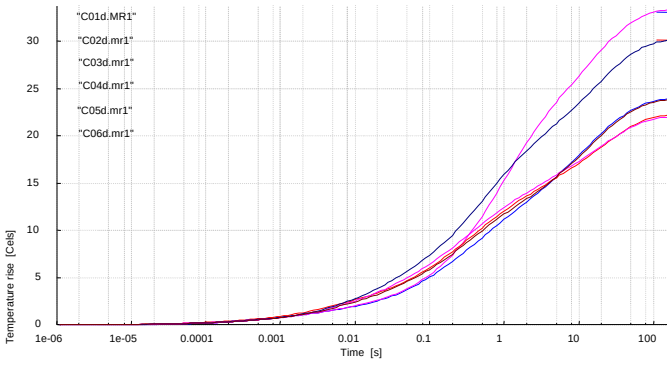

Figure 13 Measured thermal transient curves of good and bad devices

We demonstrated the method on a series of power transistors, each mounted on a copper base plate and fixed on a larger aluminum mounting plate (Figure 12). The measurement took place on a water cooled cold plate in order to assure faster transients. In case of measuring on cold plate 300s was enough to reach the steady state. The measurement was done by *T3Ster*® [9], with the resolution of 1µs and 0.012 °C. [11] The measured transient curves are presented in Figure 13.

Examining the measured transient curves we can notice differences, but the conventional comparison of these curves is rather difficult. The comparison of the *structure functions* (Figure 11) is much easier.

It can be noticed that there are characteristic differences between the presented functions. To understand these differences let us discuss first the differential structure function of the device C08, which shows the smallest steady-

state R_{th} value and so was selected as the 'good' reference device (Figure 14). The left-hand side of the curve of Figure 14 refers to the chip, the right hand end to the cold plate, arrow **4** shows this point**.** The value read on the horizontal axis gives the steady state thermal resistance between the chip and the cold plate; it is 3.2 K/W.
The zigzagged beginning of the curve shows the presence of some noise, but an average K=0.1 value can be considered.

In case of silicon material this is equivalent to a 19.7 mm^2 cross sectional area, which is in fact the area of the chip. The next peak, designated as **1** refers to the heat capacitance of the transistor case, determined by the dominant heat capacitance of the copper base plate of the case. The next peak **2** is the heat capacitance of the copper island of the mounting plate, peak **3** is the heat capacitance of the mounting plate itself.

After locating these characteristic points, the partial thermal resistance values can be read from the figure. The thermal resistance between the **1-2** points is about 0.6 K/W, this is the thermal resistance component of the transistor soldering. Between points **2-3** the thermal resistance of the plastic coating can be read, in our case this is about 1.3 K/W. The thermal resistance between the mounting plate and the cold plate determines the distance between points **3** and **4**. Comparing the structure function of C02 to the reference function (Figure 15.) we notice that at C02 a characteristic minimum is visible at the right hand side of peak **2**, and the thermal resistance to the next plateau is much (2.5 times) higher. This suggests the presence of a soldering problem.

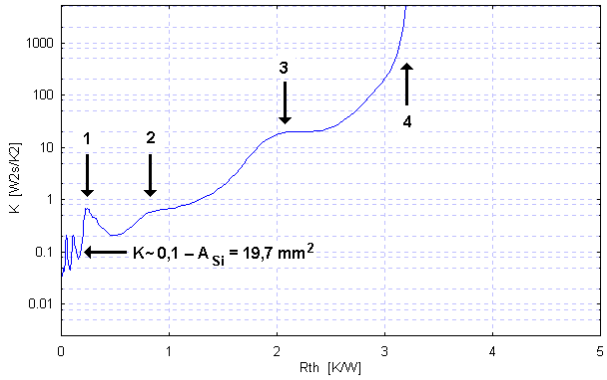

Figure 14 The differential structure function of the reference device. The arrows point to characteristic locations of the structure.

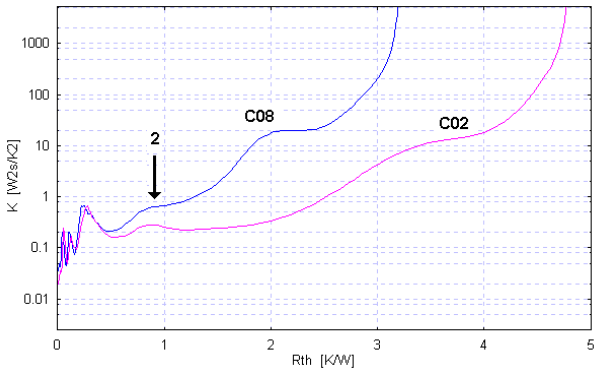

Figure 15 Comparison of the differential structure functions of C02 and C08.The shift in peak 3 suggests soldering error

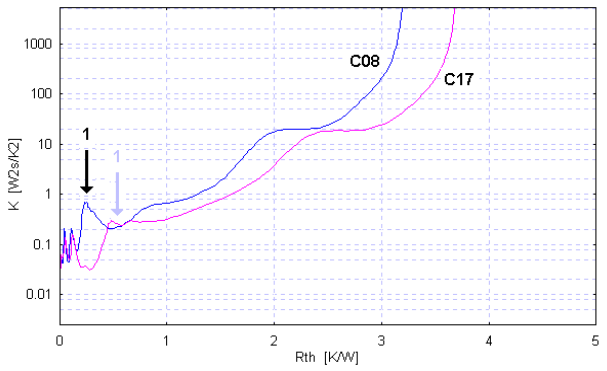

Figure 16. The differential structure function of C17 referred to the structure function of C08. The shift of peak 1 suggests die attach failure

The differential structure function of the C17 device is presented in Figure 16. At the C17 device the peak **1** and the part of the curve right from the peak is shifted to the right with a value of 0.4 K/W. This means the presence of an extra thermal resistance between the chip and the copper platform of the case, which indicates that the chip is not attached to the platform appropriately.

It is important to note that these problems can be observed already on the measured transient curves. Examining the measured transient curves we can notice that the measured curves of both devices are running above the nominal curves with about 20-25% in the 0.1-0.2 sec range of the transient measurements. This is a very important experience, suggesting that die attach failures can be detected by short transient measurements offering the possibility of using the method even for in-line testing. Soldering errors of the module can be recognized from steady state thermal resistance measurements as well, but such measurements are much more time consuming. We found however that steady state thermal resistance measurements can be approximated by short transient measurements. In the present example the steady state was reached in about 300 sec but all the problematic devices could be detected already with a 10-30 sec transient measurement. The closer is the failure to the chip itself the shorter is the time needed to detect it.

The new tools

Thermal transient tester

As a response to market demands a successful thermal transient tester equipment named *T3Ster*® has been designed at MicReD. *T3Ster*® is an excellent tool for controlling and evaluating up-to-date package measurements as suggested above due to its important features:

a) Computer controlled measurement and evaluation

A user-friendly measurement control program supports controlling high precision measurements and executing all evaluation steps discussed above

b) Multi-channel architecture

Thermal coupling effects play a very important role in the temperature dependence of packages. These can be well predicted if we know the values of the thermal transfer impedances at the significant package locations, and use these values in electro-thermal simulation. Reflecting the growing demand for simultaneous temperature measurements at a number of locations on the sample, *T3Ster*® has modular multi-channel architecture. Up to 8 measuring channels work independently but synchronically, under common control and timing. This allows using several temperature sensors (diode or resistor type sensors, thermocouples and IR one-point sensors) at the same time, enabling measuring thermal coupling effects of MCMs or PW boards, tracing cold-plate temperature changes during transients etc.

c) High resolution, accuracy and sensitivity

The previously described evaluation methods require high-resolution, accurate, noise-free recordings of the thermal time responses. For this reason, the performance of *T3Ster*® has been raised to a level that is outstanding in the thermal domain. The time resolution of the sampling is 1 µs in time, , which can be reduced to 0.5 µs using a stroboscopic method. After fast and noise-free amplifiers the precise A/D architecture provides 12 bit resolution,. thus the LSB value in the lowest range is 0.012 mV. If a diode sensor is used, this corresponds to about 0.006 ºC in temperature. As opposed to other products high sensitivity can be achieved while the noise of the measurement channels is less than the LSB value, providing a 70 dB signal-to-noise ratio.

d) Digital input level compensation

The usual semiconductor temperature sensors provide a small temperature-dependent voltage change on the top of a larger voltage bias. The special architecture of the input amplifier allows digitally controlled compensation while maintaining differential input. Using this feature the software executes the compensation automatically. The range of the compensation extends to ±5 V, in order to cover the usual V_T values of power MOS transistors.

e) Add-on options

A number of hardware add-on options facilitates package measurements, including computer controlled thermostat for device calibration, pre-amplifiers for thermocouples and one-point IR sensors, a power booster unit which can raise the switched power driving capability to up to 1000 W, as well as control of thermal test chips.
For more details see [13],[14],[15].

Thermal test chips

Thermal test chips are devices to support the thermal characterization of IC packages and packaging technologies. TIMA and MicReD produce a set of actual test chips as well as IP designs of a scaleable size, starting from 2x2mm^2 (*TMC9*) through 6x6mm^2 (*TMC81*) up to a size of 24x24 mm^2, to cover the widest possible field of applications.

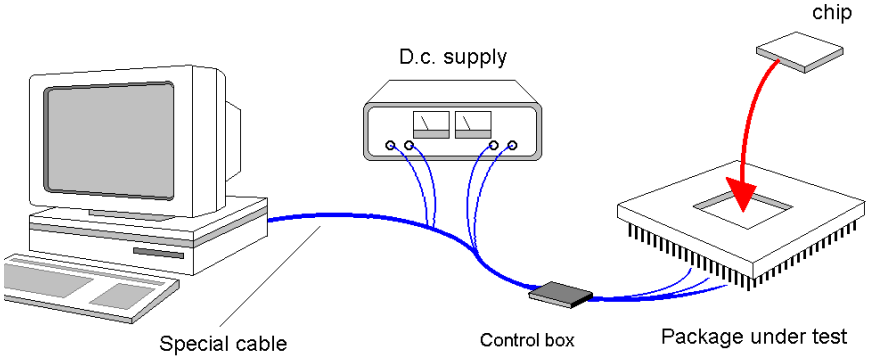

Figure 17. Stand-alone testing with thermal test chips

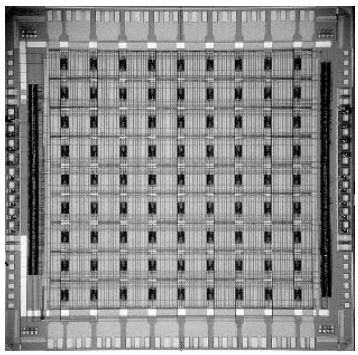

Figure 18. Micro-photograph of the TMC81 chip

These chips conform to international standards JEDEC JESD 51-4, IEEE 1149.1 .

Besides being accessories of *T3Ster®*, thermal test chips can be used as autonomous measurement units with a simple control (Figure 17). The time resolution of the sampling is 300 μs in time, and 10-11 bit in voltage in this stand-alone mode. In combination with the *T3Ster®* the accuracy described in paragraph c) above can be achieved

For more details see [16].

Conclusions

The NID method based evaluation of the measured heating curves reveals a large amount of information about the measured physical structure. The provided structure functions give the possibility to detect die attach failures or soldering inaccuracies, besides deriving material parameters. These theoretical advantages can be exploited only with high precision and noise free thermal transient measurements that require either thermal test equipment or thermal test chips of unprecedented sensitivity and accuracy, and stable and accurate mathematical evaluation methods.

Acknowledgement

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References

1. B.S. Siegal: “Measuring thermal resistance is the key to a cool semiconductor”, *Electronics*, Vol. 51. pp. 121-126, 1978.
2. V. Székely and Tran Van Bien: “Fine structure of heat flow path in semiconductor devices: a measurement and identification method”, *Solid-State Electronics*, V.31, pp. 1363-1368 (1988)
3. J.W. Sofia: “Analysis of thermal transient data with synthetized dynamic models for semi-conductor devices”, *IEEE Trans. on Comp. Pack. & Manuf.* V.18, No.1. pp. 39-47 (1995)
4. G. Oliveti, A. Piccirillo and P.E. Bagnoli: "Analysis of laser diode thermal properties with spatial resolution by means of the TRAIT method", *Microelectronics Journal*, V.28, No.3. pp.293-300 (1997)
5. V. Székely, “On the representation of infinite-length distributed RC one-ports”, *IEEE Trans. on Circuits and Systems*, Vol.38. pp.711–719, 1991.
6. E.N.Protonotarios, O.Wing: "Theory of nonuniform RC lines", *IEEE Trans. on Circuit Theory*, V.14, No.1, pp. 2-12 (1967)
7. V. Székely, M. Rencz: "Thermal Dynamics and the Time Constant Domain", *IEEE Trans. On Components and Packaging Technologies*, Vol.23, No.3, pp 687-594 (2000)
8. V. Székely: “A New Evaluation Method of Thermal Transient Measurement Results”, *Microelectronics Journal*, Vol. 28, No. 3, pp. 277-292, 1997
9. http://www.micred.com/t3ster.html
10. M. Rencz, V. Székely: “A generic method for thermal multiport model generation of IC packages” , *SEMI-THERM XVII*, San Jose, CA, USA, March 20-22, 2001, Proceedings pp 145-152
11. M.Rencz, V.Székely: “Determining partial thermal resistances in a heat flow path with the help of transient measurements”, *THERMINIC Workshop,*, Sept.24-27, Paris, France, 2001,Proceedings pp 250-255
12. V.Székely, M.Rencz, S.Török, S.Ress, B.Vizy: “Experiments on effective thermal conductivity measurements”, *Proceedings of the 6th THERMINIC Workshop*, 24-27 Sept. 2000, Budapest, pp 26-30
13. M.Rencz, V.Székely: “Dynamic thermal multiport modeling of IC packages”, Accepted to the *IEEE Transactions on Components and Packaging Technologies, Sept.2001*
14. M.Rencz, V.Székely, A.Poppe, G.Farkas, B.Courtois: ”New tools and methods for the thermal transient testing of packages”, *HD International 2001*. Santa Clara, CA, USA, April 18-20. 2001, Proceedings pp 268-273
15. V.Székely, M.Rencz,L.Pohl: “Novelties in the theory and practice of thermal transient measurements”, *THERMINIC Workshop*, Sept.24-27, Paris, France, 2001,Proceedings pp 239-244
16. A.Poppe, G. Farkas, M. Rencz, Zs. Benedek, L. Pohl, V. Székely, K. Torki, S. Mir, B. Courtois: “Design issues of a multi functional intelligent thermal test die”, Proceedings of the *SEMI-THERM XVII*, San Jose, CA, USA, March 20-22, 2001