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Layout error detection on Printed Circuit Boards (PCB) and the optimization of an emulated digital CNN-UM architecture (CASTLE)

Ph.D. thesis

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I. Introduction

A Cellular Neural Network Universal Machine (CNN-UM) [16], [17] is a stored program analog microprocessor array where the tiny nonlinear processors are interconnected locally.

The general CNN [3] is a 2-, 3-, or n-dimensional array of mainly identical dynamical systems, called cells, which satisfy two properties:

- most interactions are local within a finite radius *r*, and
- all state variables are continuous valued signals.

The CNN-UM architecture can be implemented in analog VLSI, in an emulated digital way, or by a software simulator. The operation of the digital emulated CNN-UMs is faster than the software solutions. The digital emulated CNN-UM can be implemented on VIRTEX FPGA [37], [38] or with ASIC design [46], [53].

If there are analog CNN cells in the array, we get the fastest CNN-UMs. It is the analog CNN-UM [20], [21], [22], [23], [24]. These solutions are the fastest but are inaccurate. Therefore, which can solve partial different equations too. The different programs are called analogic algorithms. The elementary instructions of a CNN program is a template execution. The size of templates is usually 3*3 (theoretically n*n).

At present the computing power of the analog CNN-UM is $3*10^{12}$ Teraops (10^{12} op/s). The CNN-UM is universal in Turing sense. So whatever algorithms are solved with this neural processor-array. The CNN is a local by connected array and is usually 2 dimensional (2D), therefore, the CNN-UM is initable for solving 2D tasks problems (e.g. image-processing applications).

The algorithm designers met different difficulties in using CNN-UMs. The first is one of them is that only 3*3 templates can be implemented on CNN-UMs. The another problem is inaccuracy. I had to answer these problems too. We can use 5*5 or n*n templates without template decomposition [1], [2], [13] if a re-configurable architecture is used that I review in Chapter 5 of my dissertation. We can keep our hands on accuracy if we use emulated digital CNN-UMs but the speed of the algorithms decreases. The speed can significantly be increased by pipeline technique [1], [2], [7]. This method is found in Chapter 5. It is important that the used silicon area should be minimal. Therefore, I presented a method that decreases the silicon area of the digital emulated CNN-UMs significantly [1], [2], [13]. If we use the method, the production cost and dissipation decreases because the circuit includes fewer FETs.

Different mistakes can be made in the course of production of printed circuit boards. Detection of these errors is not simple. The commercial systems are expensive and their usage is not trivial. I have designed analogic algorithms which detect the errors of production.

I rank my scientific work into two groups:

- error detection made during PCB production,
- optimization of an emulated digital CNN-UM (CASTLE).

First, I review two analogic algorithms, methods (error detection), then I present my optimization-results.

II. Methods used in the experiments

I examined how we can detect the different errors in the course of production of the printed circuit boards. I used Aladdin CNN-UM system [20] that was designed at CAI-HAS. We can simulate and use CNN-UMs with this system, as well as different analogic algorithms can be tested with Aladdin system.

Numerous mistakes can be made in the course of production of Printed Circuit Boards. A few type of errors may occur on the PCBs. The different short-circuits can occur because of the design or the production. These errors can be detected with my analogic algorithms [3], [4], [8], [14], [15]. These algorithms were tested by using different platforms. Measurement results are reviewed in Section 3 of my dissertation.

I have used heuristic methods.

I examined in the course of my research how can an emulated digital CNN-UM (CASTLE) be optimized according to speed, silicon area and dissipation. In my research I touched upon template-neighborhood [1], [8] too.

I used Magic [53], Cadence [54], Foundation Base [37], [38] systems and V-SIM VHDL simulator in my experiment.

A logical processor was completed with technology of AMS [47] (Austria MicroSystem). The technology with 0.35 μm-es CMOS has three metal-layers and a polysilicon. The problem of problem is solved for the case black&white input images. The templates belong to the uncompled class. I have made experiments on the chip.

III. Summary of the main results

Thesis 1 [3], [4], [8], [11], [14], [15]

The thesis deals with the detection of errors which occur in the course of the production of PCBs (Printed Circuit Board).

I have given two analogic algorithms which are able to detect these errors.

My analogic CNN algorithms can process (by using a 64*64 CNN-UM) $4*10^6$ – $0.3*10^6$ pixels/s and the best traditional system works at an order of magnitude higher speed [3], [33] but our solution is at least two orders of magnitude cheaper.

The production of PCBs is a difficult, complex problem. In the course of the PCB some errors can occur, e.g. short-circuit misalignment error. The running time of my analogic algorithms does not depend on the size of the printed circuit board if the complete image can be downloaded on the chip. I show an experiment environment in my dissertation too.

I have tested the two algorithms on the following platforms: the 64*64 CNN-UM (ACE4K), the binary CNN-UM (CASTLE) and software simulator.

Thesis 1.1 I gave an analogic algorithm, which can detect the different short-circuit on single- or multilayer printed circuit boards [3], [4], [8]. The running time of the algorithm depends on the image size. The production or the design of the PCB or can make the mistakes. If we test a single-layer PCB, the algorithm uses three inputs and an output. The inputs are the following images: a scanned image, marker, and reference. There is a black object (PAD) on the marker image from which the binary waves are started. We search for the complete pads with waves, which pertain the selected signal. After that the logic AND function is applied between the result and the reference image. There are at least two PADs on the reference image. If there is short-circuit on the tested image, there be going to be only a PAD.

Thesis 1.2 I have given an analogic algorithm which can detect the misalignment errors in the course of production of printed circuit boards [3], [8], [11]. The running time is independent of the image-size if an analog chip is used (e.g. ACE4K). We can detect the errors of the wrong artwork film.

The algorithm has two inputs and an output. The first image is the artwork film, and the second one is the drilled PCB. The algorithm localises the positions of the errors. These errors can be seen in the output image. The running time is independent of the number of errors.

Thesis 2. [1], [2], [5], [6], [7], [9], [12], [13]

The analog CNN-UMs are used in numerous implementations. These chips are faster than the emulated digital solutions and the analog CNN-UMs have the dissipation less too. But these analog solutions are inaccurate. An emulated digital

CNN-UM architecture [5] was completed at the CAI HAS it can implement 16 3*3 templates simultaneously. In the course of processing a template can be belonged to a pixel.

The download of the templates into the chip-memory is independent on operate of the chip. The size of templates is 3*3 (nearest neighbourhood). If 12 bits accuracy is used, the maximal operation frequency of CASTLE is approximately 80 MHz [1]. I modified this emulated digital architecture so that we should get a flexible and faster solutions. The second thesis shows the new solutions of the emulated digital CNN-UM (CASTLE). The solutions were optimized according to speed, area, or dissipation.

2.1 I have proposed an emulated digital CNN-UM architecture [1], [9], [13] that implements 3*3 or 5*5 templates in unit time. It is a universal re-configurable architecture. The operation speed of the architecture is equal to the speed of the original CASTLE with 3*3 [5], [12]. I have already presented two optimization methods which provide a solution for optimization of the universal re-configurable architecture according to silicon area and operation speed. In course of the operation of the re-configurable architecture we can change the size of used templates.

2.2 I have proposed a method by which the operation speed of an emulated digital CNN-UM (CASTLE) was increased significantly.

I have given two solutions which use the pipeline technique [1], [2], [7], [13]. The temporary registers are put among the multipliers and the adders only when the first method is used [43], [45]. Such a way the operation speed has been doubled.

In the second solution the temporary registers are put into the multipliers and the adders. The new operation speed is tenfold, the maximal operation frequency is approximately 1GHz [7].

The control and memory management of the original architecture had to be reshaped so that we could use the pipeline-method in the emulated digital CNN-UMs. The operation speed is approximately 1GHz, therefore, I recommended a new architecture. There are an arithmetic core and five independent local memories in the new architecture. We can capital of the operation speed with this new architecture. I showed the clock-frequency (1GHz) can be used certainly.

2.3 I have proposed an emulated digital CNN-UM arithmetic core where the silicon area is decreased with 30% [1], [2], [13]. The arithmetic unit uses only 3*3 templates.

The solution was optimized according to the used templates. If we use the symmetric templates [35], the operation speed is not changed, it will be equal to the speed of the original CASTLE architecture. The running time increases two times if arbitrary templates are used.

I have proposed such an arithmetic core where we use symmetrical and arbitrary templates because an analogic algorithm can include arbitrary templates too [35].

I have given connect of the used templates and the running time yet.

IV. Applications

The majority of research themes dealt within the dissertation is related to well-defined applications or can potentially be used in solutions employing the CNN technology.

Numerous problems can be solved with the CNN (Cellular Nonlinear Network). It is an enormous breakthrough that the first analog CNN-UMs have been published. The analog chips are very fast but, unfortunately, these CNN-UMs are sensitive to the different noise and their accuracy is wrong. Therefore an emulated digital CNN-UM solution (CASTLE) was designed at the CAI HAS (Computer and Automation Research Institute, Hungarian Academy of Sciences). This solution is slower than the analog chip. The analog and the emulated digital CNN-UMs have a further disadvantage that they can implement only 3*3 templates.

The CNN-UMs can be applied to the different error-detection in the production of the PCB (Printed Circuit Board). The bibliography deals with the detection of different errors. We can use my two analogic algorithms (short-circuit and misalignment error detection) in production of the PCB because my algorithms can be operated in real-time. So the different errors can be found during the production. At present the AOIs (Automatic Optical Inspection) are available in trade but they are expensive and difficult to use [30], [31], [32]. My layout error detection algorithms were tested on real life examples of a PCB production company, and regarding these examples the algorithms detected 100 % of errors. Testing our algorithms on a large number of problems will be done in the near future and based on the experience, a detailed statistical analysis can be made.

It is an important question how our solution refers in price/performance to the best AOI systems. My analogic CNN algorithms can process (by using a 64*64 CNN-UM) $4*10^6$ – $0.3*10^6$ pixels/s and the best traditional system works at an order of magnitude higher speed [3], [33] but our solution is at least two order of magnitude cheaper.

I propose an emulated digital architecture (CASTLE) in my dissertation. This emulated digital CNN-UM [5] (CASTLE) architecture was published few years ago.

The emulated digital CNN-UM can be used as a Partial Differential Equation computing unit (PDE engine). Special features of the CASTLE architecture are very useful in this application area, namely, the variable accuracy or space variant linear and non-linear template options, etc. On the other hand the CASTLE architecture supports the analysis of multilayer CNN structures. For example: in analysis of different CNN models of biology or physics.

Some modified, extended CASTLE architectures are shown in my dissertation. These new architectures are optimized and analized according to the silicon area, operating speed, and power dissipation.

The CNN can be programmed with different templates. In most cases the size of a template is 3*3. There are problems, which cannot be solved with the nearest neighbourhood templates. New architectures [6] are proposed which provide usage of 3*3 and 5*5 templates with the re-configurable arithmetic cores.

If we use symmetrical templates [7], the silicon area may be decreased significantly. A new emulated digital CNN architecture is shown which implements

arbitrary templates (optimized to silicon area).

The original CASTLE arithmetic unit was accelerated by pipe-lining technique [8]. With this method the operation speed of the emulated digital CNN-UM has been increased remarkably (~ 10 times) with very insignificant changes to the silicon area. This operation speed is equal to the speed of the analog CNN-UMs.

V. The author's publications

Journals, SCI periodicals

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[15] **T. Hidvégi**, and P. Szolgay, “Misalignment Error Detection in Printed Circuit Board Fabrication Using an Analogic CNN algorithm” DNS-11-2000, MTA-SZTAKI, Budapest, 2000

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