A Millimeter Wave PLL Oscillator for Optical Receivers

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Abstract. The design and experimental investigations of a harmonic microwave oscillator is presented. The transistor oscillator was designed to operate at the fundamental frequency with high third harmonic output. The final goal is to utilize the constructed circuit in a combined millimeter-wave / optical system for picocell applications presented below.

I. Introduction

Optical generation of millimeter waves is relevant for many practical applications, and there is an increasing demand for higher and higher carrier frequencies. However, millimeter-wave generation is very expensive and complex by the known and used methods.

In the new approach instead of transmitting the millimeter-wave signal, one of its subharmonic is optically transmitted and at the reception side the millimeter-wave is generated utilizing the subharmonic signal as a reference frequency. The main advantage of this system is the simplicity and the relative low cost [1]. The block diagram of this system is shown in Fig.1.

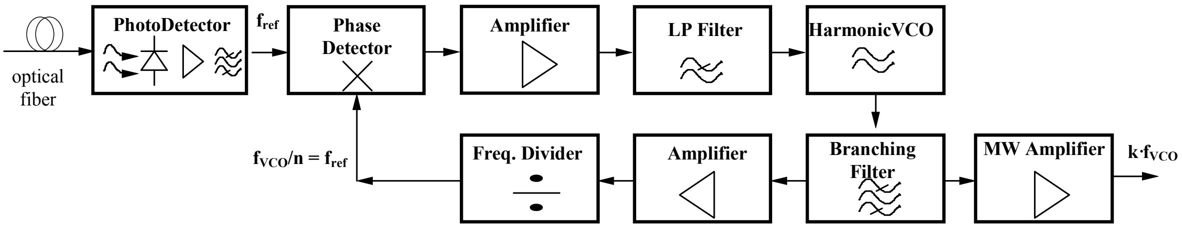

Fig. 1. Block diagram of millimeter wave generation using the optically transmitted reference

A harmonic Voltage Controlled Oscillator (VCO) is used with a fundamental oscillation frequency around $n \cdot f_{ref}$. This frequency is divided before comparing to the optically transmitted reference signal (f_{ref}) in the phase detector. The error signal is amplified, filtered and used to control the harmonic VCO frequency. One of the harmonic frequencies $k \cdot f_{VCO}$ is coupled out of the oscillator and utilized after proper amplification.

The most important device of the system is the harmonic VCO. The output power at fundamental frequency and at the selected mm-wave harmonic frequency must be optimum.

II. Oscillator design principles

Two well-known linear methods, the negative conductance and the maximum instability oscillator design method were applied in the calculations [2].

When a load is connected to a negative impedance (active device) and start-up conditions are satisfied a current starts to flow through the circuit at the frequency where the imaginary parts of both impedances cancel each other. If the instantaneous RF voltage of the active device (V_N) is larger than the instantaneous RF voltage of the load (V_L), oscillation will start when DC bias is applied to the device:

$$\left|\mathrm{V_N}\right| > \left|\mathrm{V_L}\right| . \tag{1}$$

So the oscillation start-up condition is to satisfy the condition of (Eq.2) :

$$\left|\mathrm{R_N}\right|_{t=0} > \left|\mathrm{R_L}\right| , \tag{2}$$

where the respective differential resistances are compared for the nonlinear device and the load.

The oscillation amplitude will increase and the value of the negative resistance will change until a steady oscillation is achieved. Kirchoff's voltage law can be applied (the negative resistance is in series with the load impedance):

$$\left(\mathrm{Z_N} + \mathrm{Z_L}\right)\mathrm{I} = \mathrm{ZI} = 0 \qquad \text{where} \qquad \mathrm{Z} = \mathrm{Z_N} + \mathrm{Z_L} \tag{3}$$

Since I is not equal to zero this equation is satisfied only if $Z = R + jX = 0$. Eq. (3) can be separated into real and imaginary part. That is both the real and imaginary parts must be zero. Since $\mathrm{Re}\{Z_L\}$ is greater than zero, $\mathrm{Re}\{Z_N\}$ must be less than zero, so the oscillation condition is : $-R_N = R_L$. The oscillation frequency is determined by the equation $X = 0$, that is the load reactance is the negative of the device reactance [3].

Regarding the maximum instability method an active two-port loaded by passive impedances can be considered. The input reflection coefficient of a transistor loaded by Z_L at the transistor output is given by

$$\Gamma_{\mathrm{in}} = \mathrm{S_{11}} + \frac{\mathrm{S_{12}S_{21}}\Gamma_{\mathrm{L}}}{1 - \mathrm{S_{22}}\Gamma_{\mathrm{L}}} \quad , \tag{4}$$

where $\Gamma_{\mathrm{L}} = \dfrac{\mathrm{Z_L} - \mathrm{Z_0}}{\mathrm{Z_L} + \mathrm{Z_0}}$. (Z_0 denotes the characteristic impedance.) The potential oscillation condition is $|\Gamma_{\mathrm{in}}| \geq 1$.

III. Common gate oscillator design

As an initial step of the design the Siemens CFY 15 MESFET was modeled with parameter extraction using the S-parameter data. The small signal equivalent circuit elements are : $g_m = 29.3$ mS, C_{GS}=0.45 pF, C_{DS} = 0.18 pF, C_{DG} = 0.012 pF, R_{DS} = 220 Ω, R_i=8Ω (I_{DS}= 10 mA, U_{DS} = 4V). The most nonlinear element is the transconductance g_m, which is bias dependent (g_m= 41mS at I_{DS}= 30 mA, U_{DS}= 4 V).

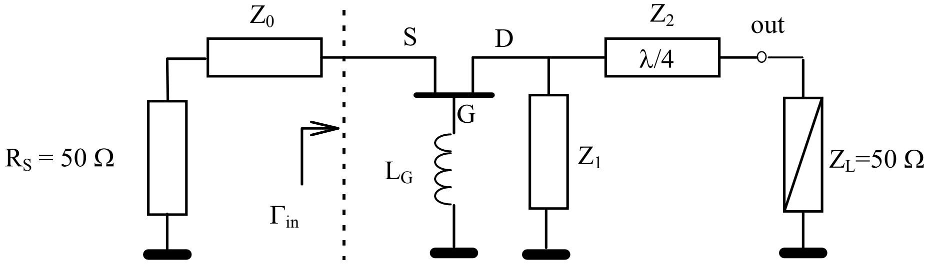

Fig. 2. Simplified oscillator circuit

The experimental oscillator circuit has been designed in common gate structure. This topology provides high negative resistance of R_N in (2) in a wide frequency band, therefore it is ideal for VCO applications. The simplified VCO circuit is shown in Fig 2.

The embedding network was designed using the maximum instability method [4] The reflection of Γ_{in} at the transistor source port according to (4) was maximized by the proper selection of the drain resonant circuit including the 50 Ω termination. The calculated source input reflection is shown in Fig. 3.

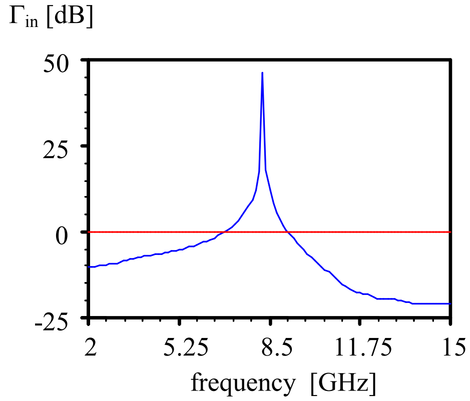

Fig. 3. Simulated Γ_{IN} of the VCO

Now the problem is to determine whether the impedances Z_L and Z_S corresponding to Γ_L and Γ_S respectively can be realized in microstrip technology without using extremely small or large strip widths.

The oscillation condition has been verified by series of simulation using HP-MDS [5] on the simplified structure. Then the topology was completed with the drain and gate biasing network, this final topology comprising the bias circuits was simulated.

IV. Measurements

The oscillator was constructed in hybrid integrated microstrip technology on Duroid substrate [6] and the circuit was tested at different transistor operating points. Fig. 4 shows the measured power spectra at the fundamental and at

the third harmonic. The frequency tuning range is plotted in Fig. 5 for the fundamental and for the third harmonic signal. Fig. 6 shows the amplitude of the first and third harmonic as a function of the gate and drain bias voltages.

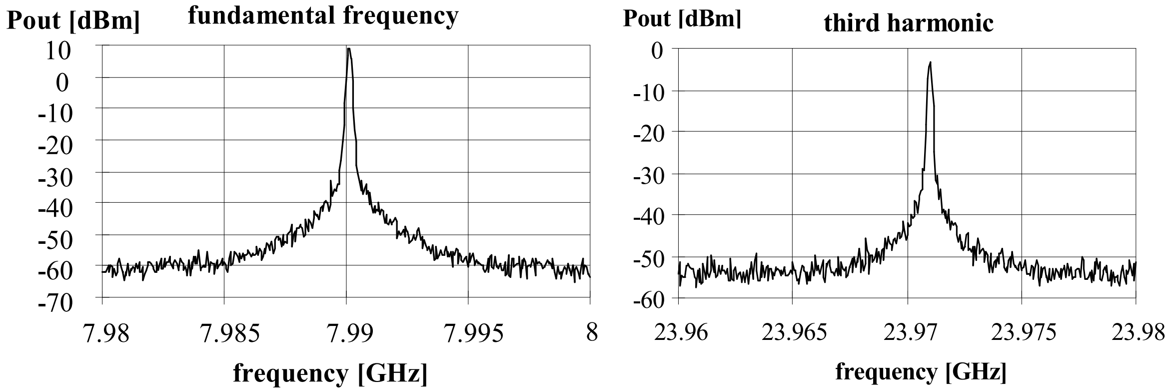

Fig. 4. Oscillator power spectra a.) at fundamental b.) at third harmonic

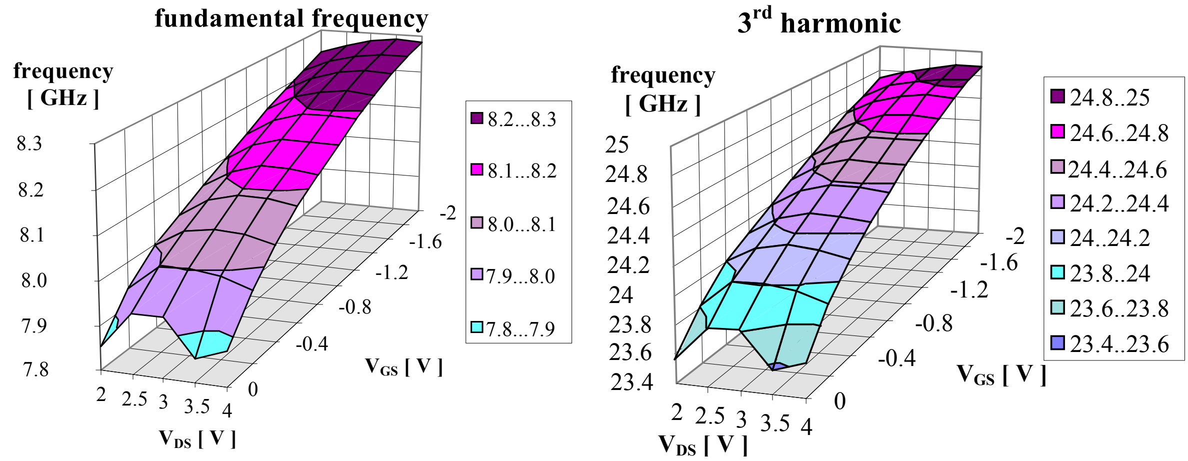

Fig. 5. Frequency tuning range versus gate & drain bias : a.) fundamental b.) third harmonic

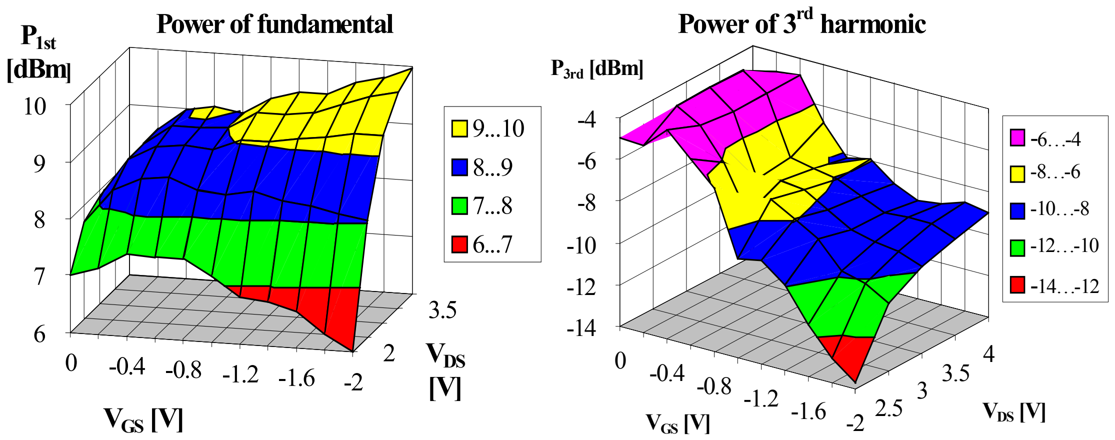

Fig. 6. a.) Oscillator power at fundamental frequency b.) at third harmonic

Acknowledgments

The authors thank I.Máté and E.Nényei at TKI Rt, for their help in the construction of the experimental oscillator circuits. The work was financed by 'OTKA' the Hungarian National Foundation for Research (projects: No. T017295, F024113), and by the 'FRANS, Fiber to Radio ATM Network Systems' research programme of the European Union.

References

[1] Tibor Berceli: "A new approach for optical millimeter wave generation utilizing locking techniques", *digest of the IEEE MTT-S conference*, Denver, USA, June, 1997.

[2] Tibor Berceli: *Nonlinear Active Microwave Circuits*, Elsevier Science Publishers, Amsterdam, Netherlands and Akadémiai Kiadó, Budapest, Hungary, 1987.

[3] Robert Soares: *GaAs MESFET Circuit Design*, Artech House Inc. 1988.

[4] Christian Gentili: *Microwave Amplifiers and Oscillators*, North Oxford Academic Publishers Ltd., 1987.

[5] Hewlett Packard: *MDS : Microwave Design System,* Software User's Manual, 1990.

[6] István Kása: *Microwave Integrated Circuits*, Elsevier Science Publishers, Amsterdam, Netherlands Akadémiai Kiadó, Budapest, Hungary, 1991.