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Optimization of Power Quality Improving Control Strategies for Grid Connected Converters

Ph. D. Thesis

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Declaration

The content of this thesis is a product of the author's original work except where explicitly stated otherwise. This thesis is submitted in fulfillment of the requirements for the PhD degree at Budapest University of Technology and Economics.

Nyilatkozat

Alulírott Futó András kijelentem, hogy ezt a doktori értekezést magam készítettem, és abban csak a megadott forrásokat használtam fel. Minden olyan részt, amelyet szó szerint, vagy azonos tartalomban, de átfogalmazva más forrásból átvettem, egyértelműen, a forrás megadásával megjelöltem. Ez az értekezés a Budapesti Műszaki és Gazdaságtudományi Egyetem által adományozható PhD fokozat megszerzési feltételeinek teljesítése érdekében kerül benyújtásra.

Budapest, 2021. _____

(Futó András)

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Andras Futo

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Abstract

Ever increasing numbers of PWM modulated voltage source inverter (VSI) based power electronic converters are connected to our modern electrical grid. The large number and high combined total power of electronic converters connected to the grid have necessitated ever stricter standards regarding harmonic emissions. Harmonic emission problems can be mitigated using hardware based solutions like changing the power circuit topology of the converter, increasing the size of filtering components, or using faster semiconductors and increased switching frequency. As opposed to this, my research was aimed at finding new cost effective software methods to reduce emissions and help to comply with grid compatibility standards of traditional two-level PWM modulated VSI converters without costly hardware modifications. My further goal was to verify the operation of the novel methods by computer simulation and also to conduct tests and measurements on actual hardware wherever possible. During my research, I have also developed a novel simulation method which has enabled a fast but more realistic simulation of two-level PWM modulated VSI converters.

The researches are primarily based on time domain analysis. As a first step, the waveform diagrams for the switching states were drawn for each thesis. Then the systems of equations required for the control method were determined and solved. This was especially complicated for the third thesis, where the symbolic mathematical toolbox of MATLAB was also used.

After creating the actual algorithms, each algorithm was tested using off-line computer simulation. The Matlab Simulink environment was used for this purpose in all cases. In the second thesis, Simulink was also used to generate a discrete time system which became translatable to an FPGA based real-time HIL simulator.

Published results related to the first and the second theses are dependent on offline simulation only. In case of the third thesis, the described method was tested on a low power model originally developed for educational purposes. Further measurements were also performed on the rectifier stage of a DC electric car fast charger unit at PROCON Drivesystem Ltd.

Összefoglaló

Modern elektromos hálózatainkra egyre nagyobb számban csatlakoznak impulzus szélesség (PWM) modulált feszültséginverter (VSI) alapú teljesítményelektronikai átalakítók. Az inverterek nagy száma és nagy együttes beépített teljesítménye a harmonikus kibocsátás szigorú szabályozását tette szükségessé. A berendezések harmonikus kibocsátásának problémája hardveres megoldásokkal is kezelhető a főáramköri topológia megváltoztatásával, a szűrőköri alkatrészek méretének növelésével, vagy gyorsabb félvezetők és nagyobb kapcsolási frekvencia használatával. Kutatásaim során ezzel ellentétben költséghatékony tisztán szoftveres eljárások keresésével foglalkoztam, melyekkel költséges hardveres változtatások nélkül is csökkenthető a harmonikus kibocsátás és elérhető a hálózati szabványoknak való megfelelés hagyományos kétszintű PWM modulált feszültséginverterek esetén. További célom volt az új irányítási módszerek számítógépes szimulációval történő ellenőrzése, valamint lehetőség szerint tényleges hardveren történő tesztelése és bemérése. Kutatásaim során egy új szimulációs eljárást is kidolgoztam, mely kétszintű feszültséginverterek korábbiaknál gyorsabb és valósághűbb szimulációjára alkalmas.

A tézisek nagyrészt időtartománybeli vizsgálatokon alapulnak. Első lépésben a tézisekben az egyes kapcsolási állapotokra jellemző jelalakokat rajzoltam fel. Ez után a kompenzációhoz szükséges egyenletrendszereket írtam fel és oldottam meg. Ez a lépés a harmadik tézis esetén különösen bonyolult volt, itt a MATLAB szimbolikus matematikai eszköztárát is használtam.

Az algoritmusok kidolgozása után midegyiket off-line számítógépes szimulációval ellenőriztem. Ehhez a Matlab Simulink környezetét használtam. A második tézis esetében a Simulink környezetet egy diszkrét idejű modell megalkotásához is felhasználtam, ami így a továbbiakban FPGA alapú valós idejű HIL szimulátorok készítésére is alkalmassá vált.

Az első és a második tézisekkel kapcsolatban publikált eredményeket csak off-line szimulációval ellenőriztem. A harmadik tézis esetében az eredmények egy kisteljesítményű, eredetileg oktatási célra kifejlesztett inverteren is bemutatásra kerültek. Ehhez kapcsolódóan a PROCON Hajtástechnika Kft jóvoltából további méréseket is végeztem egy egyenáramú elektromos autó gyorstöltő berendezés aktív egyenirányító fokozatán.

List of Symbols and Abbreviations

This chapter aims to clarify the symbols and abbreviations specific to the topic.

Symbol	Meaning
AC	alternating current
Ap	linear amplification of discrete PI controller
BLDC	brushless DC drive
CBSM	Carrier Based Subharmonic Modulation
C_H	junction capacitance of the high side switching transistor
CISPR	*Comité International Spécial des Perturbations Radioélectriques* (CISPR; English: International Special Committee on Radio Interference)
C_L	junction capacitance of the low side switching transistor
CPLD	complex programmable logic device
CPU	central processing unit
C_{sim}	simulated capacitance
CSV	comma separated values
D	theoretical duty ratio of the high side switching transistor for a phase leg operating with no delays and dead time. Equal to Udc divided by the desired average phase leg voltage U_{br}
D'	compensated theoretical duty ratio (see D)
D*	same as D, theoretical duty ratio of the high side switching transistor for a phase leg operating with no delays and dead time. Equal to Udc divided by the desired average phase leg voltage U_{br}
D_1, D_2, D_3	theoretical duty ratios of the high side switching transistors in a three phase inverter
D_{12}, D_{13}, D_{23}	line duty ratios, e.g. $D_{12} = D_1 - D_2$, $D_{13} = D_1 - D_3$, $D_{23} = D_2 - D_3$
DC	direct current
DCM	discontinuous conduction mode
DIR	direction of the triangular carrier, +1 for increasing or -1 for decreasing
D_{LL1}	line duty ratio between the two phases undergoing a type-1 transition
D_{LL2}	line duty ratio between the two phases undergoing a type-2 transition
dphi	the phase angle region used for a modified flat-top transition
DPWM	discontinuous pulse width modulation
D_P	duty ratio in phase P
D_s	value of the next smaller duty ratio
DSP	digital signal processor
DVR	dynamic voltage restorer
D_x	duty ratio of phase leg x.
D_Z	zero sequence component of duty ratio

EMC	electromagnetic compatibility
EMF	electromotive force, no-load induced voltage
f_1	fundamental frequency
f_C	carrier frequency
FFT	fast fourier transform
FPGA	field programmable gate array
f_{sw}	switching frequency, for CBSM it is same as f_C
HIL	Hardware-in-the-Loop
i_1, i_2, i_3 or i_a, i_b, i_c	phase currents on a three phase grid
i_{12}, i_{23}, i_{13}	same as i_{C12}, i_{C23}, i_{C13}
I_{AV}	average current
I_{AV2}	average current in the period of the zero sequence change (for flat-top modulation)
i_{C12}, i_{C23}, i_{C13}	line currents of AC-side output filtering capacitors in delta configuration
IEC	International Electrotechnical Commission
IGBT	insulated gate bipolar transistor
I_f	fundamental component of current
I_L	output filter inductor current, equal to phase leg output current
$I_{L,av}$ or I_{Lav}	average output filter inductor current, equal to phase current
I_{lim}	maximum possible change of current during one simulation time step
i_{off}	value of an output filter inductor current at the beginning of effective dead time
$I_{P,av}$	average inductor current or phase current for phase P
L	output filter inductor
L_{disc}	value of output filtering inductor for nearly zero current
MOSFET	metal oxide semiconductor field effect transistor
N	artificial neutral point of a three phase grid, made by connecting three identical impedances to the grid in star configuration
n	whole number, number of switching periuds utilized for a modified flat-top transition
NPC	neutral point clamped topology
PLL	phase locked loop
PV	photovoltaic
PWM	pulse width modulation
PWM_H	control signal for the high side switching transistor T_H in a phase leg
PWM_L	control signal for the low side switching transistor T_L in a phase leg
q(t)	charge of a capacitor as function of time
Q_{13}	charge of the C_{13} output filtering capacitor in delta configuration
Q_{AV}	average charge of a delta connected output filtering capacitor
RPM	rotations per minute
R_{sim}	simulated resistance
sgn()	sign function, returns +1 for positive and -1 for negative arguments

S_P	switch state in the switching sequence table for phase P. 0 for free-wheeling, +1 if the phase leg is connected to u_{dc+} and -1 if connected to u_{dc-}
STATCOM	static synchronous compensator
SW_H	same as T_H
SW_L	same as T_L
T	duration of one switching period, equal to the period of the triangular carrier
t_1	time until switch-off in another phase leg after the beginning of effective dead time.
t_{1a}	same as t_1 but limited to t_d maximum
t_d, t_{deff}	effective dead time: both switching transistors in a phase leg are switched OFF during t_d
T_H	high side switcing transistor
t_H	same as t_{HI}
THD	total harmonic distortion
t_{HI}	ON-time of the high side switching transistor
Ti	integration time of discrete PI controller
t_k	begin time of the k-th state of the switching sequence table, measured from the begining of the half period.
T_L	low side switcing transistor
t_L	same as t_{LO}
t_{LO}	ON-time of the low side switching transistor
t_{SIM_RESP}	simulation response time, same as loop delay or control system dead time
t_{step}	simulation time step, same as Ts
t_z	time required for an output filter inductor current to decrease to zero after the beginning of effective dead time.
$t_{z,a1}$	Same as t_z for a1 type transitions
$t_{z,a2}$	Same as t_z for a2 type transitions
$t_{z,b1}$	Same as t_z for b1 type transitions
$t_{z,b2}$	Same as t_z for b2 type transitions
t_{zs}	time to zero value t_z corrected for a switch-over in another phase leg
U_1, U_2	possible voltage values of the filter inductor L
u_1, u_2, u_3 or u_a, u_b, u_c	phase-to-neutral voltages of a three phase grid
U_b, U_{br}	phase leg voltage, also called bridge voltage; voltage between phase leg output and the center (0V) point of the DC bus.
U_{bP}	phase leg voltage (same as U_b) for phase P of a multiphase inverter
u_{C12}, u_{C23}, u_{C13}	line voltages of AC-side output filtering capacitors in delta configuration
Udc	Full DC bus voltage
u_{dc-}	voltage of the negative DC rail to the center (0V) point of the DC bus.
u_{dc+}	voltage of the positive DC rail to the center (0V) point of the DC bus.
u_{err}	theoretical error of voltage Uout (same as Δu)
u_{L1}, u_{L2}, u_{L3}	voltages across three output filter inductors
u_{La1}	voltage across the filtering inductor for the phase actually under investigation for the a1 discontinuous waveform

u_{Las}	voltage across the filtering inductor for the phase actually under investigation for the a1 discontinuous waveform after switch-over in another phase
U_{LEG}	phase leg voltage (same as U_b) for a phase leg
u_N	zero sequence voltage between the artificial neutral point of a three phase grid and the center (0V) point on the DC bus of the inverter connected to it
u_{N1}	neutral point voltage (see u_N) before switch-over in another phase
u_{N2}	neutral point voltage (see u_N) after switch-over in another phase
u_{NC}	zero sequence voltage (see u_N) for continuous conduction
u_{ND}	zero sequence voltage (see u_N) for discontinuous conduction
u_{Ns}	neutral point voltage (see u_N) after switch-over in another phase
U_{out}	internal voltage of the load connected to the output of the inverter
VSI	voltage source inverter
ZVS	zero voltage switching
α	phase angle
α_step	the discrete time controller steps α by this ammount in every switching half-period
ΔD_1	required change in D_1 for compensation of type-1 flat-top transitions
ΔD_{2A}	required change in D_2 for compensation of type-2a flat-top transitions
ΔD_{2B}	required change in D_2 for compensation of type-2b flat-top transitions
Δi_{13}	peak-to-peak ripple of the line current i_{13}
ΔI_{err}	ripple of falsely simulated error current
ΔI_L	switching frequency current difference of an output filter inductor between switch-over points with the fundamental current component removed. Equal to switching frequency ripple current in single phase inverters or DC/DC converters
$\Delta I_{L\ tot}$	same as a ΔI_L but also includes fundamental current component
ΔI_{LH}	change of inductor current in phase L during t_H includes fundamental current component.
ΔI_{LL}	change of inductor current in phase L during t_L includes fundamental current component.
ΔI_{Ln}	same as ΔI_L for phase n (see definition of ΔI_L)
ΔI_P	same as ΔI_{Ln} for phase P
ΔQ	change in the charge of a delta connected output filtering capacitor required to ensure that the average charge does not change because of the flat-top transition
Δu	theoretical error of voltage U_{out} (same as u_{err})
η	efficiency
η_2	efficiency when two phase legs are used in switching operation
η_3	efficiency when three phase legs are used in switching operation
φ_{margin}	phase margin of control loop
ω_C	crossover frequency of control loop

1. Introduction

Since the beginning of the 21th century, increasing numbers of high power electronic converters are being connected to our modern electrical grids. The widespread adaptation of power electronics is helped by low prices of processing power, highly integrated control circuitry, and cheap mass produced power semiconductor devices. IGBT and MOSFET transistor prices have fallen significantly. At current levels it is often economical to use complicated topologies taking advantage of more switching transistors, or to use electronic converters in appliances previously manufactured without them. Significant amounts of copper and magnetic core material can be spared in many applications by using electronic power converters operating above mains frequency. The advent of renewable energy and electric mobility together with the quickly falling prices of energy storage using Li-ION batteries all show that the demand for larger power converters above the 10kW mark will increase further in the foreseeable future.

Utility scale solar generation was enabled by cheap inverters needed to supply DC photovoltaic generation to three phase AC grids, and was accelerated by the decreasing prices of photovoltaic panels. As shown in Figure 1, the installed PV generation has increased in every year since 2010, while the 2019 estimated global generation from photovoltaic sources was in the 120 to 140 GW range according to [1].

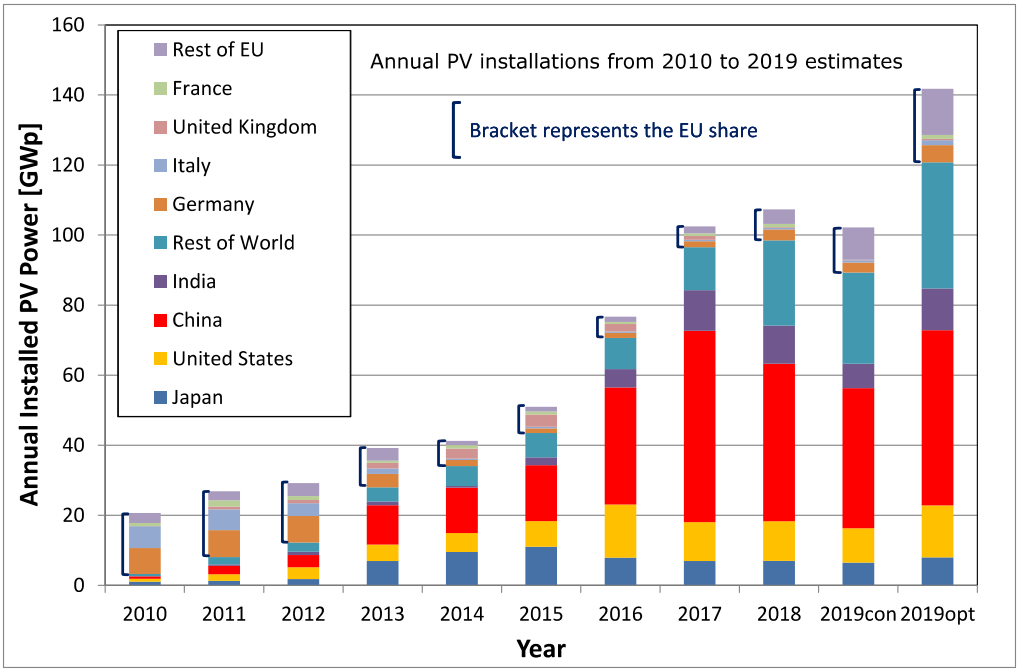
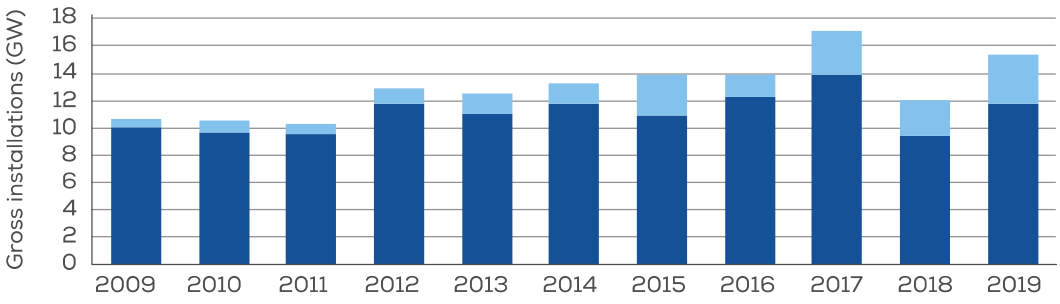


Figure 1. Annual PV installations from 2010 to 2019 estimates. Source: [1]

Wind generation also greatly profits from the use of power converters, as advanced variable speed wind turbines capable of operating at a wide range of wind speeds are being continuously installed, as shown in Figure 2. Most of these use doubly fed asynchronous generators with partially rated converters or permanent magnet generators using fully rated converters. Both require inverters to interface the grid.



	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019
Offshore	0.6	0.9	0.8	1.2	1.5	1.5	3.0	1.6	3.2	2.7	3.6
Onshore	10.0	9.6	9.5	11.7	11.0	11.7	10.9	12.3	13.9	9.4	11.7
Total	**10.7**	**10.5**	**10.3**	**12.9**	**12.5**	**13.3**	**13.9**	**13.8**	**17.1**	**12.1**	**15.4**

Figure 2. New annual onshore and offshore wind turbine installation in Europe. Source: [2]

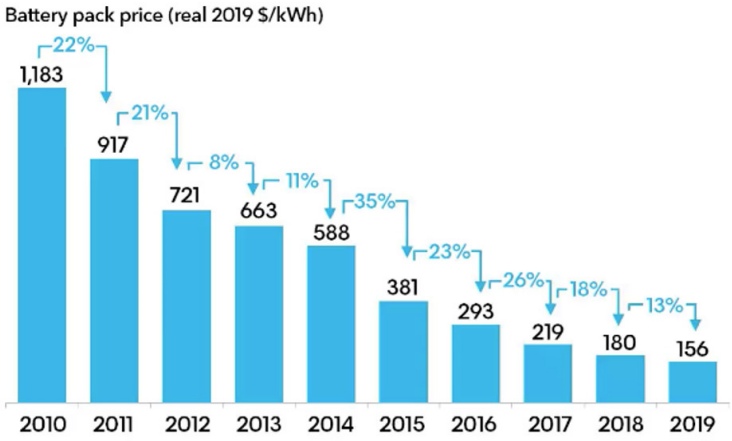


Figure 3. Lithium-ion battery price survey results: volume-weighted average. Source: [3]

The falling prices of battery storage shown in Figure 3, especially the prices of Li-ION battery cells and pack level advancements have enabled the mass production of battery electric cars. This has accelerated research in grid friendly high power rectifier technology and efficient DC/DC conversion technology. Both of them are required in on-board chargers and in DC fast chargers which are being deployed at an increasing rate as shown in Figure 4. The use of three-level topologies in these fields is also becoming widespread.

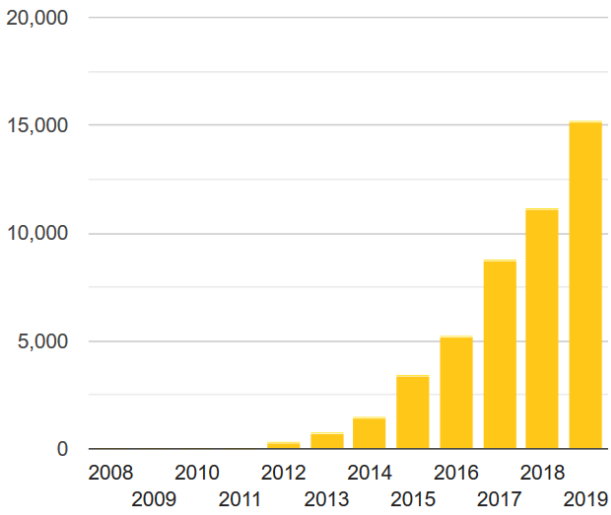


Figure 4. Total number of Fast public charging points (>22kW) in the European Union. Source: [4]

Until recently, utility-scale storage of electrical energy was mostly the field of large pumped storage hydropower installations. Using batteries in utility-scale storage is also becoming economical, in part due to extensive research and development thanks to advances in electric mobility, increasing the need for high power bidirectional grid connected converters. Grid voltage regulating devices (STATCOM, DVR) also benefit greatly from the decreasing size and price of power electronic converters, allowing continuously variable control of grid voltage, including the compensation of active- and reactive power and asymmetry on medium and low voltage grids.

As the number and total installed power of inverters and active rectifiers connected to the grid increases, the importance of maintaining power quality and electromagnetic compatibility at reasonable costs is increasing. Reactive power flow between an electronic converter and the grid can be eliminated relatively easily, but harmonic emissions are usually more problematic. Electromagnetic compatibility is often measured by the power factor or THD of the grid current, but standards define actual levels. Most current guidelines and standards, including the IEC 61000 series standards [5] of harmonic emissions only cover frequencies up to the 40^{th} harmonic [78]which is 2kHz in 50Hz countries. The CISPR standards define limits for conducted emissions starting at 150kHz but in certain applications define limits from 9kHz (for example CISPR 15 for electrical lighting). Some planned standards also use a 9kHz limit of low frequency harmonic emissions, and include frequencies up to 150 kHz [79][80].

The nonlinear behavior of power converters can be mitigated in several ways:

1. by using additional filtering circuitry
2. by using alternative power circuit topologies
3. by using additional measurement hardware for feedback
4. fully software based solutions

Methods to decrease harmonic emissions need to be power circuit specific. Using additional filtering in the power circuitry is a costly option and is not always feasible because of weight and size constraints. With the continuous development of power semiconductors and research into new more complicated topologies, the second option is often used. Line commutation based converters have been replaced by two-level PWM modulated voltage source inverters (VSI) in most applications. Their use is justified by the relatively higher power density due to smaller filter requirements. Although VSI based converters using even a simple current vector control produce significantly less low order harmonic currents when compared to line commutated converters using thyristors, nonlinearities still result in low frequency harmonic emissions. These are not attenuated by the small filters designed to eliminate switching frequency components.

With the advent of faster switching transistors came more EMC problems and additional nonlinear behavior. Modern three-level topologies have brought new challenges, as NPC bridges may have complicated dead time distortions and discontinuous conduction can be problematic in case of Vienna rectifiers [6] requiring further measures. As the number of grid connected converters increase, new cost effective solutions are required to mitigate EMC problems. Such solutions should preferably be software based, as using additional hardware even for measurement purposes adds to the costs. By using software based solutions, the size of high power filter circuits can be reduced and even the efficiency of the unit can be improved by using suitable modulation methods. The continuous development of embedded microprocessors resulting in increased and cheap computing power have enabled the application of numerous novel software based control solutions. Using modern DSPs and -in certain situations- FPGAs, control algorithms requiring more computing power can also be used in real-time applications with minimal extra cost, enabling the widespread use of even very complex control algorithms. With the decrease in the cost of computing power, an increasing need has appeared for software based solutions capable of decreasing the size, complexity and cost of power or signal level hardware components.

1.1. Objectives

During research I investigated sources of distortion in two-level VSI. The main objective of my research was to create and test control algorithms, and to support the testing of algorithms capable of decreasing harmonic emissions. It was an objective to create algorithms which do not require additional hardware apart from what is needed anyway for current vector control. I conducted research in two major fields related to sinusoidal output two-level voltage source inverters: dead time and flat-top modulation.

The first thesis discusses the causes of the distortion caused by the dead time introduced during the switch-over of two-level phase legs. My main goals in this field were to correctly describe the voltage error caused by dead-time in all operational states. I searched for occurrences of discontinuous conduction in the phase leg current. After identifying the possible waveforms and giving a method to calculate the caused voltage error, I looked for techniques which could be used to reduce their effects. My investigations began with single phase half bridge inverters. Based on the results, further research was conducted to apply them to the three phase full bridge topology widely used in the industry.

The second thesis discusses methods for the fast simulation of the distortion phenomena described in the first thesis. During this research, I focused on the execution speed of the model instead of accuracy, but I tried to find a model which is still capable of simulating discontinuous phenomena. As such, the resulting model does not simulate very high frequency transients, but it can speed up simulation significantly, and it is simple enough so that it can even be used for real-time simulation.

The third thesis discusses distortion caused by the so called 60° Flat-Top zero sequence modulation. This is also called discontinuous modulation which is used in three phase systems to enhance efficiency by decreasing the switching losses of the inverter. I have shown that this modulation results in transients in the differential output current and voltage waveforms at the steps of the zero sequence signal, resulting in harmonic emissions. The goal of the research was to reduce these emissions. It has been shown that by using a modified version of the original Flat-Top modulation, the distortion can be significantly decreased.

2. Discontinuous conduction during dead time

This thesis focuses on the compensation of distortion caused by the control dead time. For the sake of simplicity, my investigations began with single phase half bridge inverters. Such an inverter contains one phase leg which consists of a high side switching transistor T_H, high side diode D_H, and a low side transistor T_L, low side diode D_L. The phase leg needs to have an inductive load which is usually a filtering inductor L, and usually a filtering capacitor C is alos used on the AC side as shown in Figure 5. After finishing my investigation on the single phase half bridge inverter, the results were then applied to the three phase full bridge topology shown in Figure 11 as well. According to the nomenclature of Figure 5, in the rest of this chapter the middle of the DC bus will be considered zero potential, setting the positive DC rail at $U_{dc+} = U_{dc}/2$ potential and the negative at $U_{dc-} = -U_{dc}/2$.

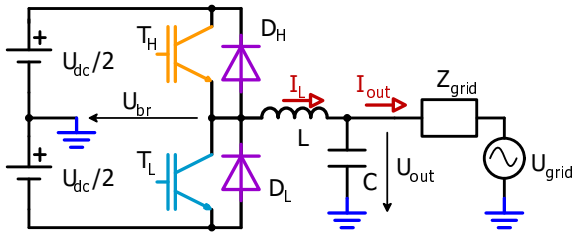


Figure 5. Single phase two-level half bridge inverter topology.

Grid connected inverters used across the industry are usually only capable of sampling the current a small number of times in each switching period. This can only be used to measure the inductor current averaged for one switching period. The average of the current is the important variable from a control system standpoint, because this is what needs to be controlled.

The output of the superimposed current controller is a desired grid-frequency component of the phase leg output voltage, let's call this $u_{br,ref}$ as it can be considered a reference. This can be described by a duty ratio D_{id} as defined in (1-1) interpreted on an ideal inverter.

$$D_{id} = \frac{u_{br,ref}}{u_{dc+} - u_{dc-}} + 0.5 \tag{1-1}$$

Such an ideal inverter would have no delays, no introduced dead time, no voltage drop or any other nonlinear behavior whatsoever, resulting in the high side switching transistor being ON for exactly $t_{HI,id} = D_{id} * T$ time in a period, and being OFF for $t_{LO,id} = (1-D_{id}) * T$. This would result in a theoretical phase leg output voltage equal to $u_{br,ref}$. as in (1-2).

$$u_{br,ref} = D_{id} \cdot u_{dc+} + (1 - D_{id}) \cdot u_{dc-} \cong \frac{1}{T} \int_0^T u_{br}(t)\ dt = u_{br,AV} \qquad (1\text{-}2)$$

If the same duty ratio is applied to a real inverter, the integral on the right side of (1-2) for the average bridge voltage $u_{br,AV}$ will not be equal to the reference voltage $u_{br,ref}$ on the left hand side. The goal of a linearization technique is to find a real duty ratio D for which $u_{br,AV}$ equals $u_{br,ref}$ with minimum error.

In voltage sourced PWM inverters, as shown in Figure 6, a small time interval called dead time is inserted during switch-over to avoid short circuit. This is called the inserted dead time, and it is marked as t_{dins} in Figure 6. During this dead time, both controllable switches in a phase leg are driven to the OFF state. Because of safety reasons, the inserted dead time t_{dins} is always more than what is needed for the switches to turn off (t_{dOFF} in Figure 6), resulting in a duration of so called effective dead time t_{deff} when both controllable switches are switched off. For sake of simplicity, effective dead time will be marked as t_d in the rest of the dissertation.

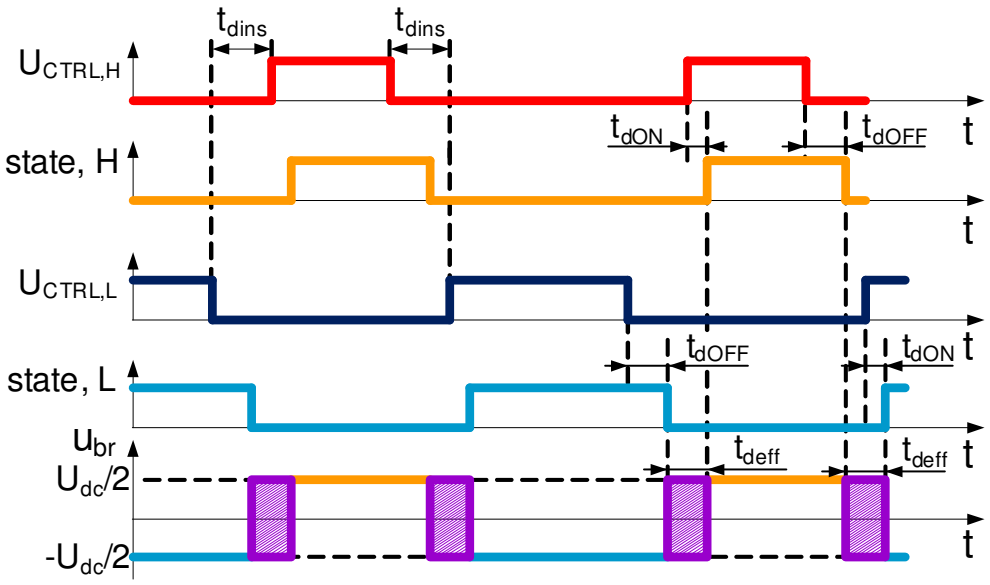


Figure 6. Control signals and states of the switching transistors in a phase leg, with the waveform of the switched voltage (bottom). Current direction dependent parts are hatched.

In this dissertation, the changes in switching states are approximated as instantaneous when calculating average phase leg output voltages. If the phase leg voltage changes quickly relative to the on- and off delays of the switches and the inserted dead time (marked as t_{dON} t_{dOFF} and t_{dins} in Figure 6, respectively), or if it rises and falls in a linear way at every switch-over, this assumption can be acceptable. The deviation between the inserted dead time and the

difference of the actual delays is the effective dead time (t_{deff} or t_d). Based on the assumption described above and on the delays marked in Figure 6, it can be calculated as follows (1-3):

$$t_d = t_{deff} = t_{dins} + t_{dON} - t_{dOFF} \tag{1-3}$$

In actual power circuits, depending on the type of semiconductor, the delay of the gate driver electronics and the rise and fall times of the power transistors depend on several factors like current, DC voltage, or temperature. As such, the actual value of the effective dead time can be estimated, but the accuracy of this estimation highly depends on the used methods. In the investigations described below and in the following sections, it was assumed that the value of the effective dead time is either constant or at least its value can be known. At this point it must be noted that testing of novel dead time compensation methods were also done with this assumption. This has greatly simplified the testing because the effectiveness of dead time compensation methods could be tested separate from delay estimation methods, but this was only possible in computer simulation. On real hardware, dead time compensation could only be tested together with a method which estimates delays and rise / fall times.

During the effective dead time, both switching transistors are switched off, and current can only flow through the antiparallel diodes. The switched point voltage of the phase leg (U_{br} in figure Figure 5a) depends on the direction of current during the effective dead time. As such, effective dead time can introduce output waveform distortion and harmonic content.

During dead time, the output voltage of the bridge U_{br} (marked with hatching in Figure 6) is determined by the direction of the output current, as this determines which of the free-wheeling diodes will conduct. This will cause an error voltage on the output which needs to be compensated for [7]. Most compensation methods, including those described in [7][8] and [9] assume that the current does not change polarity during a switching period and only compensate for large positive or negative currents. These will be called signum(I) based compensation methods. Looking at the timing diagrams in Figure 7, it can also be seen that if the current waveform has a zero crossing, then the volt-seconds lost during one switch-over from the high side transistor T_H to the low side transistor T_L (which happens while the inductor current I_L is positive) are gained back during the switch-over from T_L to T_H (this happens during negative I_L). The average error voltage caused by dead time is zero in such situations. This third state of operation happens at low currents and is taken in to account in some compensation methods like [10].

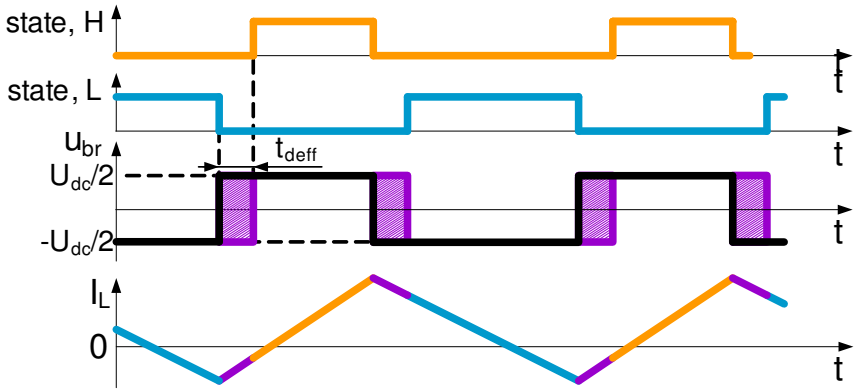


Figure 7. Cancellation of dead time effects at low currents with periodic zero crossing. The thick black line shows the resulting phase leg voltage. Diode conduction is purple.

Most methods like the ones described in [8] and [10] require the effective dead time t_d as an input parameter. The value of the effective dead time t_d depends on the on- and off delays of the switching transistors which may depend on operational conditions like output current, DC bus voltage, or even temperature, based on what type of semiconductor was used. Because of this, such methods can only be accurate if the actual value of t_d is somehow obtained. The effective dead time can be measured using dedicated hardware as described in [11] and [12] but this is expensive and the detection of current direction may also be problematic at low currents. t_d can also be obtained through identification of the system or can be calculated off-line as a function of physical parameters as in [13]. It can also be calculated during runtime using an integrator in the voltage or current feedback loop, which continuously "learns" the error voltage at the output or the value of the effective dead time [9].

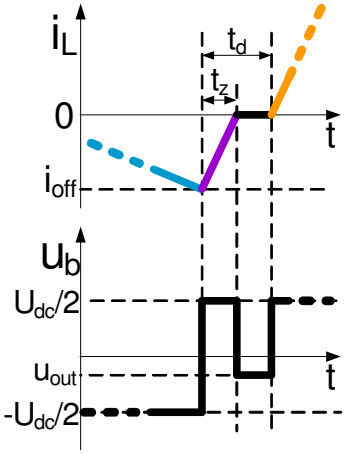
If the actual current of the L output inductor (shown in Figure 5) is close to zero at the beginning of the switch-over, it can reach zero before the end of the effective dead time. In this case, the conducting free-wheeling diode may cease to conduct and discontinuous conduction can happen [C1]. In such cases, the distortion caused by dead time will strongly depend on the operating point. The actual waveforms and the calculation of the distortion will become much more complicated.

2.1. Discontinuous conduction in single-phase half bridges

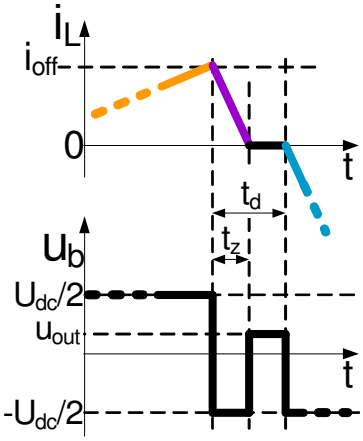
During discontinuous conduction, the U_{br} voltage of the switched point will become equal to the U_{out} internal voltage of the load connected to the output of the inverter (grid voltage, or back EMF in case of drives). Depending on the direction of the switch-over and on the sign of

the current, four possible current waveforms have been identified. The waveforms happening at $T_L \rightarrow T_H$ switch-over were named as „a“ type waveforms, and those at $T_L \rightarrow T_H$ switch-over were named as „b“ type waveforms. The a1 and b1 waveforms do contain zero crossings, but the a2 and b2 do not. All four waveforms are visible in Figure 8.

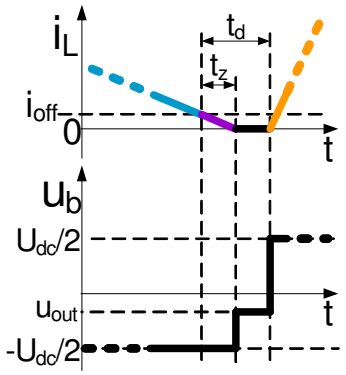
Figure 8 shows that the effects of discontinuous conduction on grid connected inverters are most significant when the positive or negative peak of the output current is close to zero for a relatively long time in each period. This often happens when the amplitude of the output current is small, but it is also possible for both effective and reactive currents. The severity of the effect depends on the operating point and on the relative value of the filtering inductor.



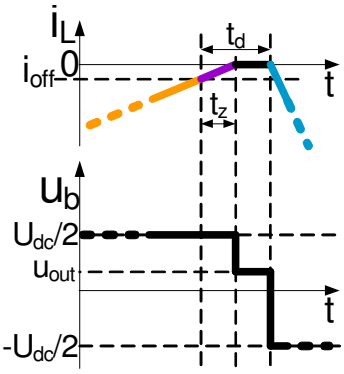
(a1) $T_L \rightarrow T_H$ switch-over, I_L direction changes



(b1) $T_H \rightarrow T_L$ switch-over, I_L dir. changes



(a2) $T_L \rightarrow T_H$ switch-over, same I_L direction



(b2) $T_H \rightarrow T_L$ switch-over, same I_L direction

Figure 8. Waveforms of discontinuous conduction during dead time for half-bridge inverters. t_d is effective dead time, t_z is time to zero current, i_{off} is current at the moment of switch-off.

The subdiagrams of Figure 8 were named after the waveforms. It can be seen that discontinuous conduction occurs if the time to zero (time required for the current to reach zero after switch-off, marked as t_z) is smaller than the effective dead time t_d. As the a and b type waveforms are analogous, the error voltage calculations have only been described for the a1 and a2 waveforms. It can be seen that the error voltage for the b1 and b2 can be expressed through the very same steps. The a1 and b1 waveforms involve zero crossing in the phase leg current; the current in the other two waveforms (a2 and b2) does not change polarity.

Error voltage for the a1 waveform

Based on the measured mean current, U_{DC} and u_{out} voltages, the value of the current at switch-off (marked I_{off}) and the time to zero t_z can be determined [C2].

On Figure 8 (a1) it can be seen that if we omit the discontinuous (zero current) interval and slide the waveform together, we will get a triangle waveform. The average of the resulting triangular current would be I_{off} plus half of the current ripple ΔI_L, but the period would be shortened by $t_d - t_z$. Taking these into account, the average current can be expressed (1-4):

$$I_{out} = I_{Lav} = \frac{1}{T}\int_0^T i_L(t)\ dt = \frac{1}{T}\left[\left(I_{off} + \frac{\Delta I_L}{2}\right)\cdot\left(T - t_d + t_z\right) + 0\cdot\left(t_d - t_z\right)\right] \qquad (1\text{-}4)$$

As already mentioned, I_{off} is the value of the inductor current at the moment of switch-off. The actual value of the current ripple ΔI_L needs to be calculated to take advantage of the equation. It can be easily calculated for continuous conduction cases. The differences in ΔI_L for discontinuous conduction will be discussed at the end of this section. The time to zero for the a1 case can be expressed (1-5):

$$t_z = \frac{-I_{off}\cdot L}{(u_{dc+} - u_{out})} \qquad (1\text{-}5)$$

Substituting (1-5) into (1-4) enables the expression of I_{off} through a quadratic equation:

$$a = \frac{L}{u_{dc+} - u_{out}} \qquad b = a\cdot\frac{\Delta I_L}{2} - T + t_d \qquad c = \frac{\Delta I_L}{2}\left(T - t_d\right) + I_{Lav}\cdot T \qquad I_{off} = \frac{-b - \sqrt{b^2 - 4ac}}{2a} \qquad (1\text{-}6)$$

The solution in (1-6) was chosen because for $t_d = 0$ this results $I_{off} = I_{Lav} + \Delta I_L / 2$ which corresponds with the ideal case. I_{off} can be used to calculate t_z. The result of this calculation can be used to decide which waveform to use. The a1 waveform shall be used for calculating the output error voltage only if $0 < t_z < t_d$. On an ideal inverter with no dead time, the high

side transistor would turn on immediately and the phase leg voltage would be the positive DC rail voltage. But instead of this, the phase leg voltage becomes u_{out} for the duration of the discontinuous conduction. The resulting error of the average phase leg voltage can be expressed using t_z from (1-5):

$$\Delta u = \frac{t_d - t_z}{T} \cdot \left(u_{out} - u_{dc+} \right) \tag{1-7}$$

This needs to be compensated to satisfy the criteria $u_{br,AV} = u_{br,ref}$ described in (1-2). It can be seen, that the above described steps for the expression of the time to zero and the error voltage for the a1 waveform can also be used to express these in case of a b1 waveform.

Error voltage in the a2 waveform

Another waveform named a2 is also shown in Figure 8. This looks similar to the a1, but it does not contain a zero crossing. Sliding this waveform together the same way as discussed for the a1 waveform results in a triangular current waveform which has a minimum value of zero. The average current can be expressed by removing the zero current interval:

$$I_{Lav} = \frac{1}{T} \int_0^T i_L(t)\ dt = \frac{1}{T} \left[\frac{\Delta I_L}{2} \cdot \left(T - t_d + t_z \right) + 0 \cdot \left(t_d - t_z \right) \right] \tag{1-8}$$

This can now be used to express the time to zero t_z:

$$t_z = \frac{2 \cdot I_{Lav} \cdot T}{\Delta I_L} - T + t_d \tag{1-9}$$

On an ideal inverter with no dead time, the high side transistor would turn on immediately and the phase leg voltage would be the positive DC rail voltage. But instead of this, the phase leg voltage becomes the negative DC rail voltage for t_z time, and u_{out} for the duration of discontinuous conduction. The resulting error of the average phase leg voltage can be expressed for the a2 waveform using t_z from (1-9):

$$\Delta u = \frac{t_d - t_z}{T} \cdot \left(u_{out} - u_{dc+} \right) + \frac{t_z}{T} \cdot \left(u_{dc-} - u_{dc+} \right) \tag{1-10}$$

The way of solution is the same for the b2 waveform as for the a2 waveform, as the waveforms are mirror images of each other. Similar to the a1 case, the calculated error voltage for the a2 waveform is also valid only if t_z is within the correct range, so $0 < t_z < t_d$ needs to

be satisfied. But this calculation can also be used to detect continuous conduction: for the a2 waveform if $I_{L,av} > 0$ and $t_z > t_d$ then there are no zero intervals in the current waveform.

Compensation of discontinuous conduction for single phase half bridge

The previous calculations were done for the b1 and the b2 waveforms the same way as for the a1 and the a2. From the four cases it is clear that if none of the t_z values satisfies $0 < t_z < t_d$ then the conduction through L is continuous. There are three such cases. For current waveforms with zero crossings but no discontinuous conduction, the net error voltage is theoretically zero. For large positive or negative currents, the resulting error voltage is independent from the magnitude of the current and the signum(I) method can be used the same way as in traditional dead time compensation methods described in [7][8] or [9]. This gives the error voltage expressed in (1-11). The actual formula can be chosen from TABLE I.

$$\Delta u = \left(u_{dc-} - u_{dc+}\right)\frac{t_d}{T}\cdot \mathrm{sgn}(I_{Lav}) \tag{1-11}$$

TABLE I ERROR VOLTAGE FOR ALL CASES

condition	***description***	***error voltage***
$I_{Lav} > 0$ and $t_{z,a2} > t_d$	continuous positive current, no zero crossings	as in (1-11)
$I_{Lav} > 0$ and $t_{z,a2} < 0$	a1 waveform	as in (1-7)
$I_{Lav} > 0$ and $0 < t_{z,a2} < t_d$	a2 waveform	as in (1-10)
$I_{Lav} < 0$ and $t_{z,b2} > t_d$	continuous negative current, no zero crossings	as in (1-11)
$I_{Lav} < 0$ and $t_{z,b2} < 0$	b1 waveform	like (1-7)
$I_{Lav} < 0$ and $0 < t_{z,b2} < t_d$	b2 waveform	like (1-10)
None of above	continuous conduction with zero crossings	zero

TABLE I shows all possible situations. In order to perform compensation, at first $t_{z,a2}$ or $t_{z,b2}$ needs to be determined based on current direction. If these are larger than t_d then the conduction is continuous and the error voltage can be determined using (1-11). In other cases, the related t_z values need to be checked, as shown by TABLE I. If one of them it is within the range between 0 and t_d, that shows that the waveform type under investigation is possible and the related error voltage formula is valid. This way, the theoretical error voltage Δu can be determined.

The error voltage characteristics for an actual inverter were drawn on Figure 9 for a constant output voltage and changing output current using the new discontinuous conduction based method, as compared to the signum(I). Comparison was also made to a simple linear interpolation based method, also called linear approximation compensation method (ACM) [13]. This method is also based on signum(I) but assumes that the error changes linearly for currents between $-\Delta I_L/2$ and $+\Delta I_L/2$. It can be seen that for large negative or positive currents the error voltage is the same with all methods. The plot for the new discontinuous method in Figure 9 was drawn for an arbitrarily chosen output voltage of $0.8\ u_{dc}/2$, of course the shape depends on the actual output voltage and changes continuously if the output voltage is sinusoidal. It is interesting to see that even though the different sections of the error voltage curve are calculated from different formulae, the resulting function is still continuous. u_{err} is the same as Δu, it is the error voltage caused by dead time.

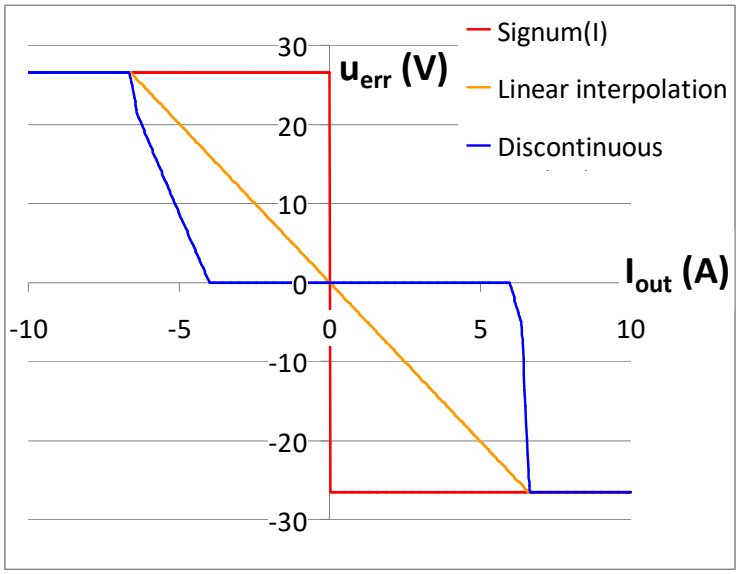


Figure 9. Error voltage as a function of current using different methods. The dark blue line shows the result with the new discontinuous conduction based method for an arbitrary output voltage of $u_{out}(t) = 0.8\ u_{dc}/2$. Parameters: u_{dc} = 664 V, L = 1 mH, T = 125 µs, t_d = 5 µs

A software based dead time compensation module can get the value of the ideal duty ratio D from the current controller. Its task is to calculate the compensated D' duty ratio which will be applied to the PWM module using inputs from sensors in the converter. For proper compensation, (1-12) has to be satisfied, where u_{err} is the error voltage caused by dead time, and it is a function of duty ratio, output voltage, and output current.

$$D \cdot \left(u_{dc+} - u_{dc-}\right) = D' \cdot \left(u_{dc+} - u_{dc-}\right) + u_{err}(D', u_{out}, I_{Lav}) \qquad (1\text{-}12)$$

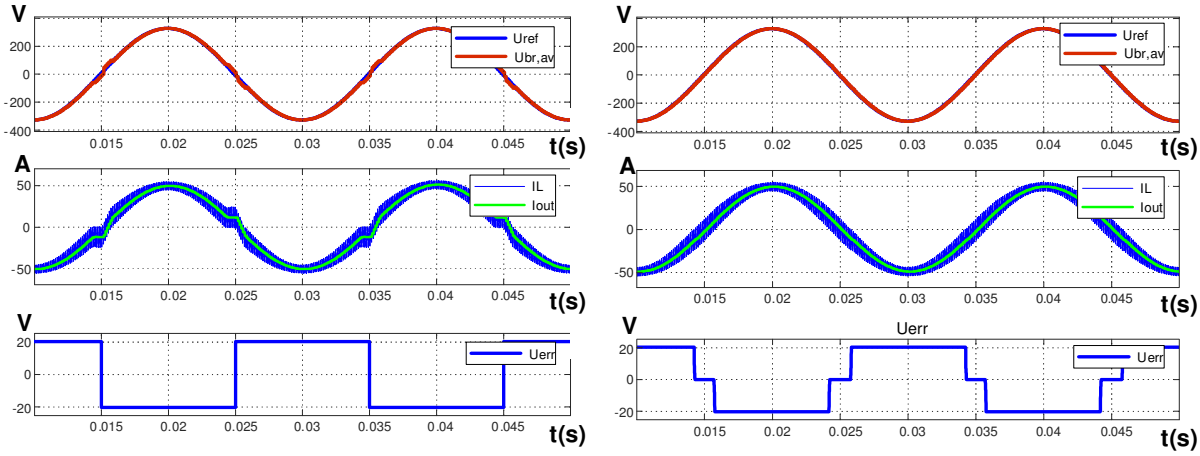
The problem is that $u_{err}(D', u_{err,} I_{Lav})$ can not be determined because D' is unknown. However, $u_{err}(D, u_{err,} I_{Lav})$ can be used as an approximation, as u_{err} is a continuous function of D on the *[0,1]* interval and the absolute value of the *(D'-D)* intervention is expected to be small. D' can be approximated as follows:

$$D' \cong D - \frac{u_{err}(D, u_{out}, I_{Lav})}{\left(u_{dc+} - u_{dc-}\right)} \tag{1-13}$$

To use the above described calculation methods for dead time compensation, we need to obtain the value of the current ripple ΔI_L. This can be easily calculated for continuous conduction cases, as seen in (1-14). If the current goes discontinuous, the current ripple will slightly decrease, but good simulation results shown in could still be achieved using the original ΔI_L value obtained for continuous conduction. The maximal error by this approximation is proportional to t_d / T. Because the effective dead time is usually in the range of 1..5 µs, this decrease in the current ripple will be always less then 10% for all useful switching frequencies, and for most cases it will be less then 5%.

$$\Delta I_L = \frac{\left(u_{dc+} - u_{dc-}\right) \cdot D \cdot T}{L} \tag{1-14}$$

To evaluate the effectiveness of the new compensation method, a simplified simulator of the circuit on Figure 5 has been built in Matlab Simulink [C2]. The filter inductor L was simulated as a series LR element. The grid together with the filter capacitor C was treated as



a: current direction or Signum(I) method b: new discontinuous method

Figure 10. Dead time compensation methods simulated on open-loop controlled half-bridge. Parameters: u_{grid} = 230 V rms, u_{dc} = 664 V, L = 1 mH, R = 65.1 mΩ T = 125 µs, t_d = 3 µs

an ideal voltage source. No current controller was used in the simulation as this would have reduced the dead time effects. The desired inverter output voltage (input D value for the compensator) was calculated so that the voltage drop on the filter inductor would cause the desired output current if the operation of the inverter is completely linear.

a shows the simulation results for a signum(I) based compensator for comparison. The average bridge output voltage $u_{br,av}$ deviates from the voltage reference $u_{br,ref}$ near the zero crossings of the low current waveform, and the resulting current waveform becomes seriously distorted at low currents. The discontinuous based dead time compensator applies a more accurate compensating voltage (u_{err}). As seen in b, the resulting current waveform is much more sinusoidal.

New scientific result – Thesis 1

Based on theoretical analysis and simulations, the following can be stated as thesis 1:

I have shown that discontinuous conduction can happen during effective dead time in single phase half-bridge inverters. I have identified the waveforms of discontinuous conduction during dead time. I have defined a method for estimating the error in the output voltage of a phase leg. I have shown that this estimation can be used for partial analytical compensation of the error in single phase half bridge inverters.

2.2. Discontinuous conduction in three-phase full bridges

In case of three phase inverters as shown in Figure 11, the waveforms of the phase currents are more complicated and can have multiple zero crossings within a switching period. This can happen as no neutral wire is connected to this circuit, only the three phases. Some methods are described in literature which treat low current situations separately, and are able to distinguish the current waveforms having multiple zero crossings within one period from those which do not have [13][17]. The three phase current waveforms are different for the three phase angle domains of the phase leg output voltage (sectors). Based on this approach, a DC link current ripple calculation was done in [18]. A very similar approach was used in [19] to calculate the peak-to-peak current ripple for seven phase and in [20] for three phase inverters.

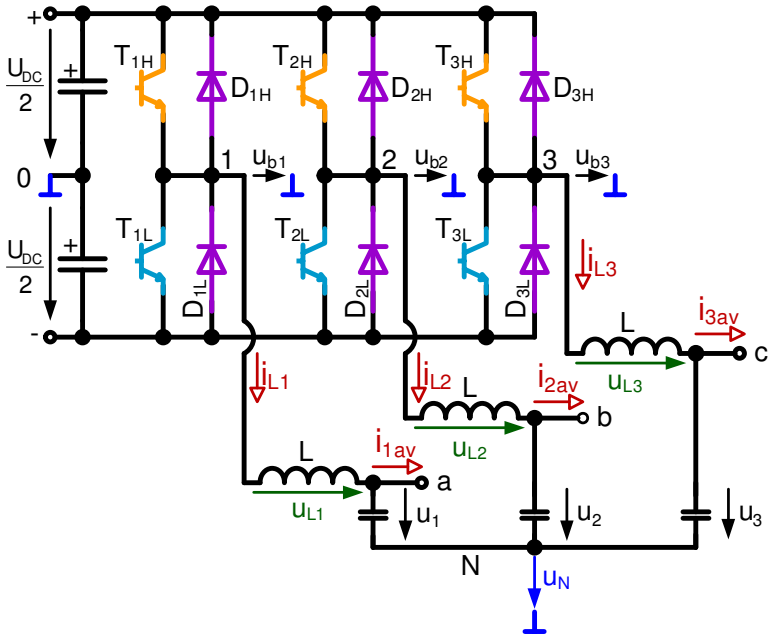


Figure 11. Three phase two-level full bridge inverter topology

To be able to build a good dead time compensator for the circuit shown in Figure 11 capable of handling low current situations well, the current values where switch-over (and dead time) occurs, need to be determined. This means that the actual current ripple value $\Delta I_{Ln}(t)$ relevant for dead time compensation has to be determined for all three phases, or at least a good approximation is required [17]. For three phase inverters, it is probably better to call the $\Delta I_{Ln}(t)$ as current difference instead of current ripple, because it is the current difference measured for a phase between the two switch-over points within a switching period and it is not equal to the peak-to-peak current ripple in all cases [C3]. As such, I will call it current difference instead of ripple in this chapter.

Three phase current waveforms and current difference calculation

The following calculations were performed for a three phase full bridge inverter with an artificial neutral at the star point of the AC capacitor bank. Because the neutral wire of the grid is not connected to the three phase full bridge inverter, the neutral point N is assumed as floating with respect to the DC bus just like shown in Figure 11. The voltages and currents follow the nomenclature of Figure 11. The phase leg voltages u_{b1} u_{b2} u_{b3} and the neutral voltage u_N are referenced to the middle potential of the DC bus shown as 0 at the middle point of the two DC capacitors in Figure 11. The grid phase voltages u_1 u_2 u_3 are referenced to the artificial neutral point N. u_{L1} u_{L2} u_{L3} are voltages across the inductors, i_{L1} i_{L2} i_{L3} are the currents of the inductors, and i_{1av} i_{2av} i_{3av} are the grid currents.

The calculations were performed for three phase continuous, triangular carrier based or centered symmetrical PWM modulation. It is assumed that each phase current is averaged between the two lower corners of the triangle carrier, and the new duty ratios are applied at the higher corners of this triangle carrier, as seen on Figure 12. The formulas below apply to all continuous modulations, but not for discontinuous ones (e.g. Flat-top). However, it can be seen that discontinuous modulations can be handled in a similar way. In a three phase system the phases can be put in order at any moment based on the duty ratio values:

$$D_1 \leq D_2 \leq D_3 \tag{1-15}$$

The voltage and current waveforms of the circuit of Figure 11 can be seen on Figure 12 in this order specified in (1-15) at an arbitrarily chosen phase angle. On this figure the three duty ratios are relatively distant, but in a real three phase system any two duty ratios might have the same value. As the neutral point of the grid (or load in case of a grid-forming inverter) is not directly connected to the DC bus, the voltage between the artificial neutral point (N on Figure 11) and the ground point of the DC bus marked with u_N will also be a time-varying voltage. This voltage can be determined at all times using circuit theory:

$$u_1 + u_2 + u_3 = 0, \quad i_{L1} + i_{L2} + i_{L3} = 0, \quad i_{1av} + i_{2av} + i_{3av} = 0, \quad u_N = \frac{u_{b1} + u_{b2} + u_{b3}}{3} \tag{1-16}$$

This results in a four-level signal for u_N which is also drawn on Figure 12. The switching frequency component of each inductor voltage is mostly determined by the potential difference between the bridge output of the phase and the neutral point. Therefore these have been plotted on Figure 12 for all phases with the average phase voltages and currents treated as constant for one switching period. From these, the current waveforms could already be drawn on Figure 12 as well. The waveforms of Figure 12 are drawn for a theoretical steady state, omitting the effect of fundamental frequency AC components, and assuming that the mean voltage across each inductor will be 0 or close to 0 for a full switching period. The effect of the fundamental harmonic was not taken into account, assuming that it changes slowly when compared to the changes at or above switching frequency. Note that the current differences ΔI_1 ΔI_2 ΔI_3 shown in Figure 12 show the difference of the current between the switch-over points of one switching period for phases 1 2 and 3 with the fundamental harmonics of the currents assumed zero. These ΔI current difference values are not necessarily equal to the peak to peak current ripples of the phases, they can be smaller as shown by the example of phase 1 in Figure 12.

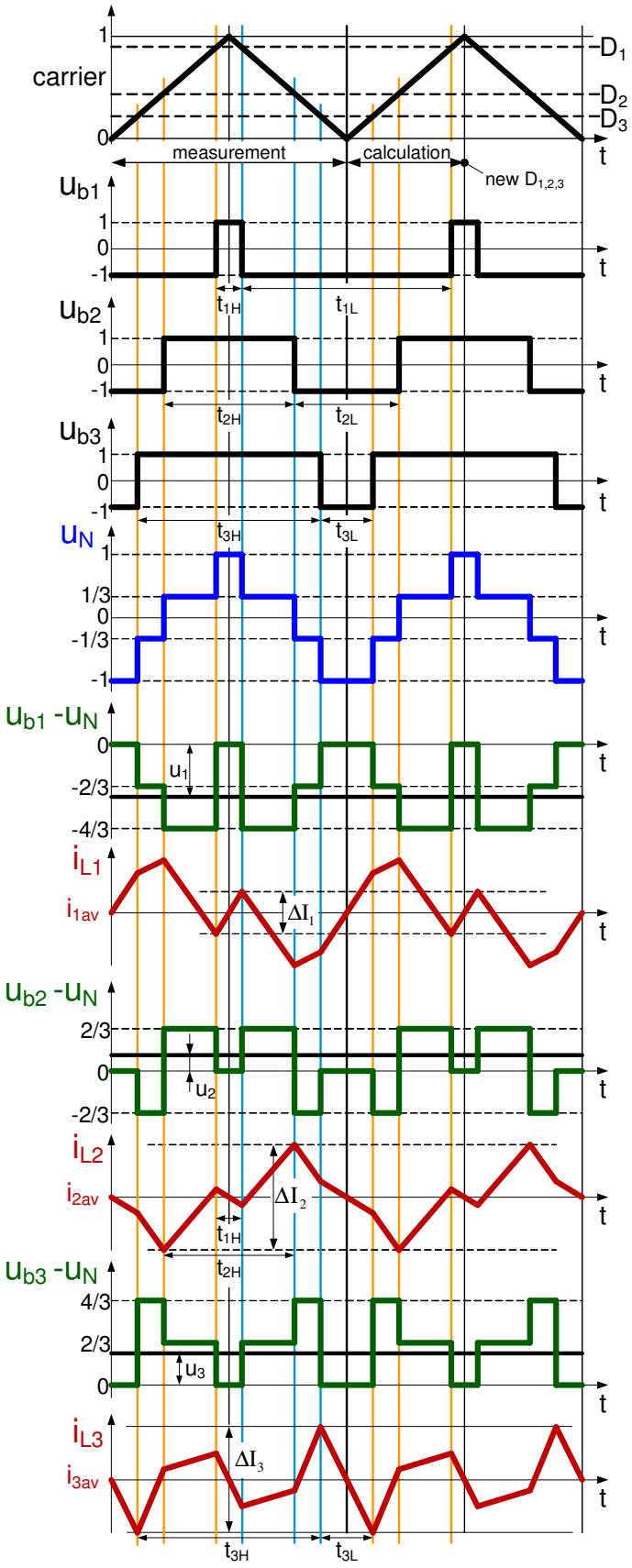


Figure 12. Control signals, voltages and currents of an ideal three phase inverter.
The fundamental components of the currents are not shown. All voltages are scaled in $U_{DC}/2$

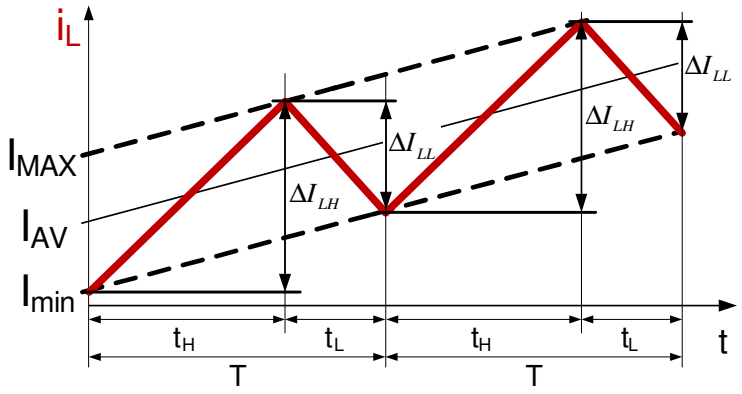


Figure 13. Different inductor current difference definitions for single phase inverter

In Figure 12, the fundamental frequency components were omitted to simplify the problem, but in reality doing so would result in a significant error. Including the fundamental components of the phase currents but assuming their slope constant for one switching period seems to be a good approximation. Figure 13 is based on this approximation and it shows that two different current difference calculations are possible for each phase. (Figure 13 only shows the waveform for a single phase standalone inverter to simplify the problem, so the changes in current slope caused by switch-over in other phase legs are not drawn). One current difference can be calculated for high phase leg output voltage (1-17), and one for low output voltage (1-18). These two are different because the output current is not DC but it also has a low frequency fundamental component which will be marked as $I_f(t)$. As mentioned earlier, the slope of the fundamental current $dI_f(t) / dt$ is assumed constant for one switching period.

$$\Delta I_{LH} = t_H \cdot \frac{dI_f(t)}{dt} + \Delta I_L \tag{1-17}$$

$$\Delta I_{LL} = t_L \cdot \frac{dI_f(t)}{dt} - \Delta I_L \tag{1-18}$$

For the actual case shown in Figure 13, $\Delta I_{LH} > 0$ and $\Delta I_{LL} < 0$. The fundamental component of the current change $dI_f(t)$ can be approximated by a linear slope, resulting in (1-19). To get the value of the current difference caused by switching (ΔI_L), the effect of fundamental harmonic has to be removed. This can be done by expressing ΔI_L from (1-20) as shown in (1-21).

$$\Delta I_{LH} + \Delta I_{LL} = T \cdot \frac{dI_f}{dt} \tag{1-19}$$

$$\Delta I_{LH} - \Delta I_{LL} = (t_H - t_L) \cdot \frac{dI_f}{dt} + 2\Delta I_L \tag{1-20}$$

$$\Delta I_L = \frac{1}{2}\left(\Delta I_{LH} - \Delta I_{LL} - \frac{t_H - t_L}{T}\left(\Delta I_{LH} + \Delta I_{LL}\right) \right) \tag{1-21}$$

As the current waveforms of the three phase inverter are symmetrical, the same calculations can also be performed for the current waveforms of Figure 12. To be able to perform these calculations, ΔI_{LH} and ΔI_{LL} need to be determined. It is important to notice, that the incoming measurement data (average current) is valid for the middle point of the previous switching period (upper corner of the triangular carrier on Figure 12). To be able to determine the distance of the switch-over current from the measured value, the slope calculated from (1-19) is also required.

As shown before, all three inductor current waveforms can be seen on Figure 12. The current difference of interest is twice the difference of the actual current at switch-over, and the average current for the period. This can be calculated in two steps. At first, the current differences (ΔI_1, ΔI_2, ΔI_3) need to be determined based on the inductor voltages and their duration. The inductor voltages can be calculated because the state of the switching transistors is known as drawn in Figure 12. Of course, the DC voltage and the grid voltages need to be measured periodically, but it is enough to measure these at switching frequency because the voltages of the capacitors can not change very fast. The base harmonic content needs to be removed from the current differences as in (1-20), and then the current difference can be obtained as in (1-21). These same steps can be seen in (1-22)-(1-25), (1-27)-(1-30), and (1-32)-(1-35) for all parts of the waveform. After the calculations, a correction is done with the slope of the fundamental harmonic to get the total current difference ΔI_{1_tot} which includes both fundamental and switching frequency components. This can be seen in (1-26), (1-31), and in (1-36). The actual formulae are given below.

1. *Calculation for the smallest duty ratio:*

$$\Delta I_{1H} = \frac{u_{L1} \cdot t_{1H}}{L} = \frac{(u_{b1} - u_N - u_1) \cdot t_{1H}}{L} = \frac{-u_1 \cdot t_{1H}}{L} \tag{1-22}$$

$$\Delta I_{1L} = \frac{\left(\frac{-2U_{DC}}{3} - u_1\right)\left(t_{1L} - t_{2L}\right) + \left(\frac{-U_{DC}}{3} - u_1\right)\left(t_{2L} - t_{3L}\right) - u_1 \cdot t_{3L}}{L} \tag{1-23}$$

$$\frac{dI_{1f}}{dt} = \frac{\Delta I_{1H} + \Delta I_{1L}}{T} \tag{1-24}$$

$$\Delta I_1 = \frac{\Delta I_{1H} - \Delta I_{1L} - \left(t_{1H} - t_{1L}\right) \cdot \frac{dI_{1f}}{dt}}{2} \tag{1-25}$$

$$\Delta I_{1\_tot} = \Delta I_{1H} = \Delta I_1 + t_{1H} \cdot \frac{dI_{1f}}{dt} \tag{1-26}$$

2. *Calculation for the middle duty ratio:*

$$\Delta I_{2H} = \frac{-u_2 \cdot t_{1H} + \left(\frac{U_{DC}}{3} - u_2\right) \cdot \left(t_{2H} - t_{1H}\right)}{L} \tag{1-27}$$

$$\Delta I_{2L} = \frac{-u_2 \cdot t_{3L} + \left(\frac{-U_{DC}}{3} - u_2\right)\left(t_{2L} - t_{3L}\right)}{L} \tag{1-28}$$

$$\frac{dI_{2f}}{dt} = \frac{\Delta I_{2H} + \Delta I_{2L}}{T} \tag{1-29}$$

$$\Delta I_2 = \frac{\Delta I_{2H} - \Delta I_{2L} - \left(t_{2H} - t_{2L}\right) \cdot \frac{dI_{2f}}{dt}}{2} \tag{1-30}$$

$$\Delta I_{2\_tot} = \Delta I_{2H} = \Delta I_2 + t_{2H} \cdot \frac{dI_{2f}}{dt} \tag{1-31}$$

3. *Calculation for the highest duty ratio:*

$$\Delta I_{3H} = \frac{\left(\frac{2U_{DC}}{3} - u_3\right)\left(t_{3H} - t_{2H}\right) + \left(\frac{U_{DC}}{3} - u_3\right)\left(t_{2H} - t_{1H}\right) - u_3 \cdot t_{1H}}{L} \tag{1-32}$$

$$\Delta I_{3L} = \frac{u_{L3} \cdot t_{3L}}{L} = \frac{(u_{b3} - u_N - u_3) \cdot t_{3L}}{L} = \frac{-u_3 \cdot t_{3L}}{L} \tag{1-33}$$

$$\frac{dI_{3f}}{dt} = \frac{\Delta I_{3H} + \Delta I_{3L}}{T} \tag{1-34}$$

$$\Delta I_3 = \frac{\Delta I_{3H} - \Delta I_{3L} - \left(t_{3H} - t_{3L}\right) \cdot \frac{dI_{3f}}{dt}}{2} \tag{1-35}$$

$$\Delta I_{3\_tot} = \Delta I_{3H} = \Delta I_3 + t_{3H} \cdot \frac{dI_{3f}}{dt} \tag{1-36}$$

Compensation of discontinuous conduction in three phase full bridges

The method of compensation is described in [J1]. To be able to perform compensation, the switching frequency component of each inductor voltage u_{L1}, u_{L2}, u_{L3} across the inductors shown in Figure 11 need to be determined for the duration of the dead-time. These can be calculated as potential differences, by subtracting the phase voltages (u_P for phase P) measured across the capacitors and the neutral point voltage (u_N) from the bridge voltages of the phase (u_{bP}). The neutral point voltage is the voltage between the star point of the capacitor bank and the middle point of the DC bus. This u_N voltage was calculated for all conduction situations in (1-16). u_N for continuous conduction will be called $u_{NC.}$. If one phase leg goes discontinuous, it will be at grid potential, and the formula will be different. The neutral voltage for such cases was named $u_{ND.}$ This can be seen for example for phase "1" in (1-37):

$$u_{NC} = \frac{u_{b1} + u_{b2} + u_{b3}}{3} \qquad u_{ND} = \frac{u_1 + u_{b2} + u_{b3}}{2} \tag{1-37}$$

The a1 waveform in a three phase full-bridge

The goal of compensation $u_{br,AV} = u_{br,ref}$ is the same as determined for the single phase half-bridge in section 2.1. The expression of the average inductor current (1-4) can also be used for one phase of a the three phase circuit:

$$I_{Pav} = \frac{1}{T}\left[\left(I_{off} + \frac{\Delta I_P}{2}\right)\cdot\left(T - t_d + t_z\right)\right] \tag{1-38}$$

However, as the inductor voltages are different, the expression of the time-to zero t_z will be more complicated than for the single phase half bridge inverter. To be able to calculate it, we need to know the voltage across the inductor in the actual P phase leg undergoing a1 type discontinuous waveform. This has been marked as u_{La1} in (1-39). u_p is the voltage of phase P.

$$t_z = \frac{-I_{off}\cdot L}{u_{La1}} \quad \text{where} \quad u_{La1} = \frac{u_{DC}}{2} - u_{NC} - u_p \tag{1-39}$$

u_{NC} can be calculated from (1-37) by substituting $u_{DC}/2$ for the voltage of the phase leg under investigation, because the output current is negative during t_z, as Figure 8 (a1) shows. From (1-38) and (1-39), I_{off} can already be expressed. This quadratic equation similar to (1-6) can be solved as in (1-40). Then t_z can be determined (1-39).

$$\left.\begin{aligned} a &= \frac{L}{u_{La1}} \\ b &= a \cdot \frac{\Delta I}{2} - T + t_d \\ c &= \frac{\Delta I_L}{2}\left(T - t_d\right) + I_{Lav} \cdot T \end{aligned}\right\} I_{off} = \frac{-b - \sqrt{b^2 - 4ac}}{2a} \tag{1-40}$$

The above calculation was based on the assumption, that u_N does not change while the current decreases to zero. This does not necessarily apply in a symmetrical voltage system, as the difference between any two duty ratios can be very small or even zero. This means, that two switch-over events can overlap. For the a1 waveform this can happen if the duty ratio of the actual phase leg under investigation is not the smallest in the order (1-15). In this case, the time between the beginning of effective dead time and the switch-off in another phase leg named t_1 needs to be calculated from (1-41) using the duty ratio D_P of the phase leg P under investigation for the a1 waveform, the next smaller duty ratio $D_S < D_P$ of another phase and the switching frequency f_s. If $t_1 < t_z$ then there is a switch-off in the phase leg with smaller duty ratio D_s. A diode will take over conduction in that phase leg after t_1 time. Thus the new u_{NC} has to be determined from (1-37) based on the direction of the current in that phase, this neutral voltage after the switch-over in the other phase will be called u_{Ns}. The resulting u_{Ns} is used in (1-42) to determine the new u_{La1} after switch-over in the other phase (in this case called u_{Las}).

$$t_1 = \frac{D_P - D_s}{2 f_s} \tag{1-41}$$

$$u_{Las} = \frac{u_{DC}}{2} - u_{NS} - u_p \tag{1-42}$$

The change in the neutral voltage will add an additional breakpoint the a1 waveform, so it will be different from the original of Figure 8 (a1). The resulting waveform was named a1s and is shown in Figure 14.

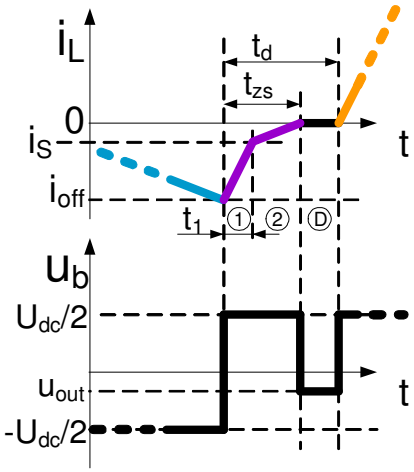


Figure 14. Waveforms of case a1 with switch-off in another phase leg during dead time (a1s)

As shown in Figure 14, the slope of the current changes after t_1 time ②. The new time-to-zero-switched value t_{zs} can be calculated the same way as t_z, based on (1-38), but (1-42) and (1-43) are needed instead of (1-39). The result of this new system of equations can be seen on (1-44).

$$t_{zs} = t_1\left(1-\frac{u_{La1}}{u_{Las}}\right)-\frac{I_{off}\cdot L}{u_{Las}} \tag{1-43}$$

$$\left.\begin{aligned} a &= \frac{L}{u_{Las}} \\ b &= a\cdot\frac{\Delta I_L}{2}-T_c+t_d-t_1\cdot\left(1-\frac{u_{La1}}{u_{Las}}\right) \\ c &= \frac{\Delta I_L}{2}\left(T-t_d+t_1\cdot\left(1-\frac{u_{La1}}{u_{Las}}\right)\right)+I_{L,av}\cdot T \end{aligned}\right\} I_{off} = \frac{-b-\sqrt{b^2-4ac}}{2a} \tag{1-44}$$

So if $t_1 < t_z$ then t_z shall be overwritten with t_{zs} calculated from (1-43). After finishing the above calculations, the resulting t_z can be checked against the range criteria $0 < t_z < t_d$ to see if the a1 case is applicable at all. If yes, then the corresponding error voltage can be determined for this case. This is done very similarly to the single phase solution described in section 2.1 for the first thesis. The main difference is in the way of determining the output voltage of the inverter during the discontinuous period. u_{ND} from (1-37) is required for this, but the three phase formula also has to be able to handle a switch-over in the next phase leg with smaller duty factor. This happens if $t_z < t_1 < t_d$. In this case, a diode will take over

conduction in that phase leg after t_1 time. Thus the new u_{ND} has to be determined from (1-37) based on the direction of the current in that phase. The error voltage formula in (1-45) for the error voltage u_{errPa1} handles this case with $t_{1a} = t_1$ substitution, but it can also be used for the basic case (no switch-over in another phase during discontinuous conduction) if $t_{1a} = t_d$ is substituted. u_{N1} and u_{N2} in the formula mean the neutral point voltages before and after the switch-over in the foreign phase, and u_p means the voltage of the actual phase (u_1, u_2 or u_3).

$$u_{errPa1} = \frac{t_{1a} - t_z}{T} \cdot \left(u_{N1} + u_p - \frac{u_{dc}}{2} \right) + \frac{t_d - t_{1a}}{T} \left(u_{N2} + u_p - \frac{u_{dc}}{2} \right) \tag{1-45}$$

Based on the above

The a2 waveform in a three phase full-bridge

Based on (1-38), the time-to-zero can be expressed as in (1-46) for the a2 waveform:

$$t_z = \frac{2 \cdot I_{L,av} \cdot T}{\Delta I_L} - T + t_d \tag{1-46}$$

The calculated error voltage for the a2 case is also valid only if the range criteria ($0 < t_z < t_d$) are satisfied. Like for the single phase case, it can also be seen that for the a2 case if $I_{L,av} > 0$ and $t_z > t_d$ then the conduction is continuous and there are no zero intervals in the current waveform. The resulting error voltage for the a2 case is expressed in (1-47). This formula is also capable of handling a switch-over in the phase with smaller D_s duty ratio during dead time, similar to (1-45). This happens if $t_z < t_1 < t_d$. If the D of the actual phase under investigation is the smallest, or if $t_1 > t_d$ then a $t_1 = t_d$ substitution can be used. For $t_1 < t_z$ then a $t_1 = t_z$ substitution gives the correct results.

$$u_{errPa2} = -u_{dc} \cdot \frac{t_z}{T} + \frac{t_1 - t_z}{T} \cdot \left(u_{N1} + u_p - \frac{u_{dc}}{2} \right) + \frac{t_d - t_1}{T} \cdot \left(u_{N2} + u_p - \frac{u_{dc}}{2} \right) \tag{1-47}$$

Compensation, simulation results

Based on the calculations shown so far, it is clear that the error voltage u_{errP} for phase P can be calculated from, and as such, is a function of the three duty ratios D_1 D_2 D_3, any two of the phase currents i_{1av} i_{2av} i_{3av} and any two of the phase voltages u_1 u_2 u_3. In the two previous subsections, the compensation was only shown for positive phase currents (for a1, a1s and a2 waveforms), but the formulae for negative currents (for b1, b1s and b2 waveforms) were deduced in a completely analogous manner and as such will not be included here. Once the

voltage error u_{errP} is known for each phase, the method of compensation for the three phase inverter is the same as for the single phase case already described in section 2.1. The modified *D'* duty cycles can be calculated based on (1-48) for each P phase:

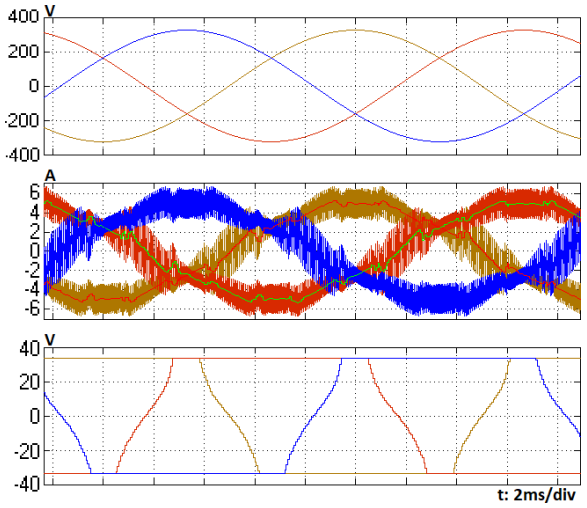
$$D_P \cdot u_{DC} = D_P^{'} \cdot u_{DC} + u_{errP}\left(D_1, D_2, D_3, u_1, u_2, i_{1av}, i_{2av}\right) \tag{1-48}$$

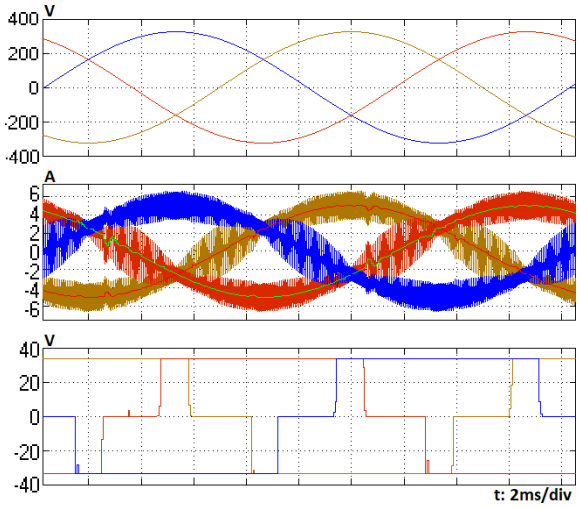
Simulation results showing the effectiveness of the solutions introduced in sub thesis 1.1 can be seen in Figure 15. For currents smaller than half of the current difference estimated using the method in [C3], the solution shown in Figure 15a uses a linearly decreasing amount of dead time compensation. Figure 15b shows simulation results using the new method which also compensates for discontinuous conduction. The simulated inverter operates on a 400V 50Hz three phase grid using DQ current vector control. The filter of the inverter was sized for 50A peak phase current, using an inductor of 5% and a resistance of 1% nominal load impedance. The control used a 16kHz triangular carrier using symmetrical / space vector control. The introduced dead time was 3μs.

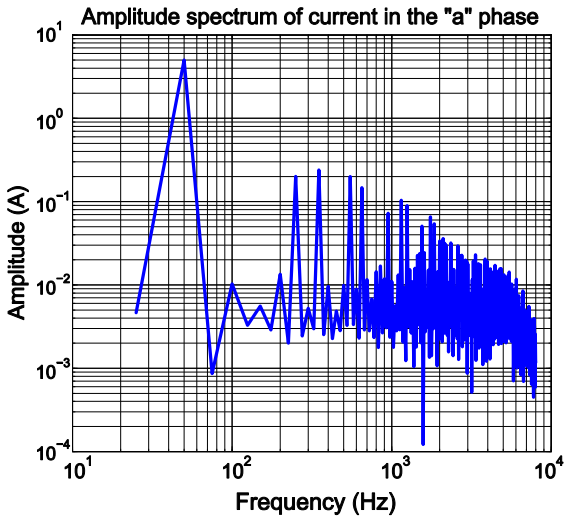
New scientific result – Sub thesis 1.1

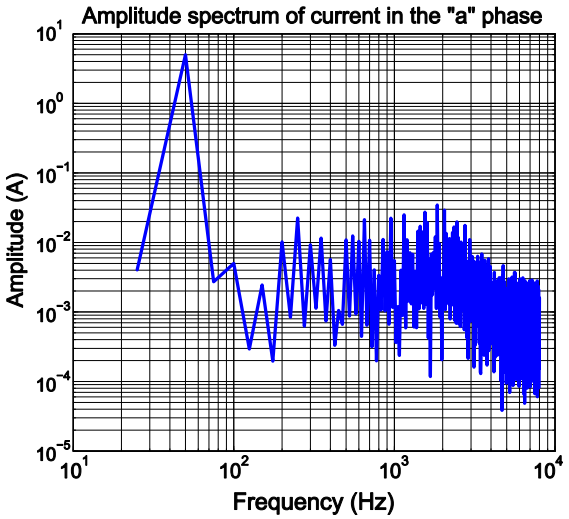
Based on theoretical analysis and simulations, the following can be stated as sub thesis 1.1:

I have shown that discontinuous conduction can happen during effective dead time in three phase full-bridge inverters. I have defined a method for forecasting the values of current ripple for the next switching period of three phase two level inverters. I have shown that by using the forecasted current ripple values it is possible to compensate for the error caused by discontinuous conduction during switching dead time. I have verified the operation of the new dead time compensation method by computer simulation.









a. Linear interpolation based method. THD = 9.3 %

b. Discontinuous compensation method THD = 2 %

Figure 15. Simulated effect of dead time compensation methods on three phase inverters. Top to bottom: grid voltage, inductor and output phase currents, output of dead time compensator, and the amplitude spectrum of one phase inductor current on the bottom. THD is calculated for one output phase current up to the 40th harmonic.

2.3. Model based dead-time compensation

The analytical method of compensation for discontinuous conduction in three phase inverters described in section 2.2 for subthesis 1.1 and in [J1] has been shown to work well in simulation. However, its execution on an actual DSP or microcontroller is problematic, as it requires high processing power for the calculation of complicated formulae and square root functions. Research was done to find a computationally simpler solution [C4].

The basic idea behind the new method is to incorporate an accurate model into the controller which is capable of modeling all switching states including both low current situations and discontinuous conduction. The inputs of such a model are the instantaneous phase currents sampled at a known time relative to the triangular carrier, the phase voltages, the direction of the triangular carrier (also marked with DIR, with values of +1 for increasing or -1 for decreasing), and the duty ratios determined by the superordinate controller for an ideal, linear system. The dead time compensator runs a model of the inverter which generates the phase currents and phase leg voltage waveforms from these inputs for the end of each switching state during a half period of the triangular carrier. For that time period it also determines the resulting volt-seconds for each phase leg. A similar approach was described in a paper by D. Schröder and R. Kennel [21] for a thyristor based DC drive. A significant difference is that for a DC drive it was relatively easy to determine the desired current waveform from the required average output current. In a three phase PWM system this is much harder, as the three phase legs affect each other through the potential of the neutral point. Because of this, the resulting voltage and current are determined instead for a given duty ratio. Intervention is done using the same approximation formula as described for thesis 1 and subthesis 1.1 in sections 2.1 and 2.2.

Operation of the model

The operation of the model can be understood based on Figure 16. The model assumes that a triangular carrier based PWM modulation is used with the duty ratios updated at both to and bottom peaks of the triangular carrier. This modulation can also be called double update PWM in certain publications. The used model splits each half period of the triangular carrier to time segments based on switching state. Calculated instaneous phase currents and the state of the semiconductor switches are available for the beginning of each iteration of steps 1-7; these are stored in the status vector as on TABLE II. This vector is initialized on startup with

the input measurement data. All initial phase leg switch states are determined by the slope or direction of the triangular carrier (DIR) as positive or negative, unless the duty ratio is so small (or large) that the last switch-over has not been finalized. In the latter case, the phase leg is assumed as free-wheeling (this has been marked as switch state 0).

The model determines the voltages across the circuit for the actual time segment, and then it determines the length of the actual time segment (the time period for which the previously calculated voltages remain valid). After this, it determines the initial currents and the switch states for the next time segment.

TABLE II THE STATUS VECTOR

time	bridge voltages			neutral voltage	inductor voltages			switch state			phase currents		
t_k	u_{b1}	u_{b2}	u_{b3}	u_N	u_{L1}	u_{L2}	u_{L3}	S_1	S_2	S_3	I_1	I_2	I_3

A time segment can end two ways. In most cases a switch-over happens, which can be detected based on the switching sequence table (TABLE III) which has to be previously sorted based on time. The other possibility is that a free-wheeling phase leg (in switch state 0) goes discontinuous. This decision is made in step 5 in Figure 16. If a switch-over happens, then the new switching state is loaded, and the switching sequence table is stepped one row further (i.e. the first row is removed).

TABLE III THE SWITCHING SEQUENCE TABLE

time	phase	next state
t_{s1}	1	0
$t_{s1} + t_d$	1	-DIR
t_{s2}	2	0
$t_{s2} + t_d$	2	-DIR
t_{s3}	3	0
$t_{s3} + t_d$	3	-DIR
T/2	don't care	don't care

The iterations are continued until the last element is cleared from the switching sequence table. The last state always lasts until the end of the half period (T/2). To detect this, a dummy element may also be added to the table, as in TABLE III to make sure that the output contains

all volt-seconds for the corresponding half switching period. During initialization, it is made sure that this dummy element is the last in the list (i.e. all time values are smaller).

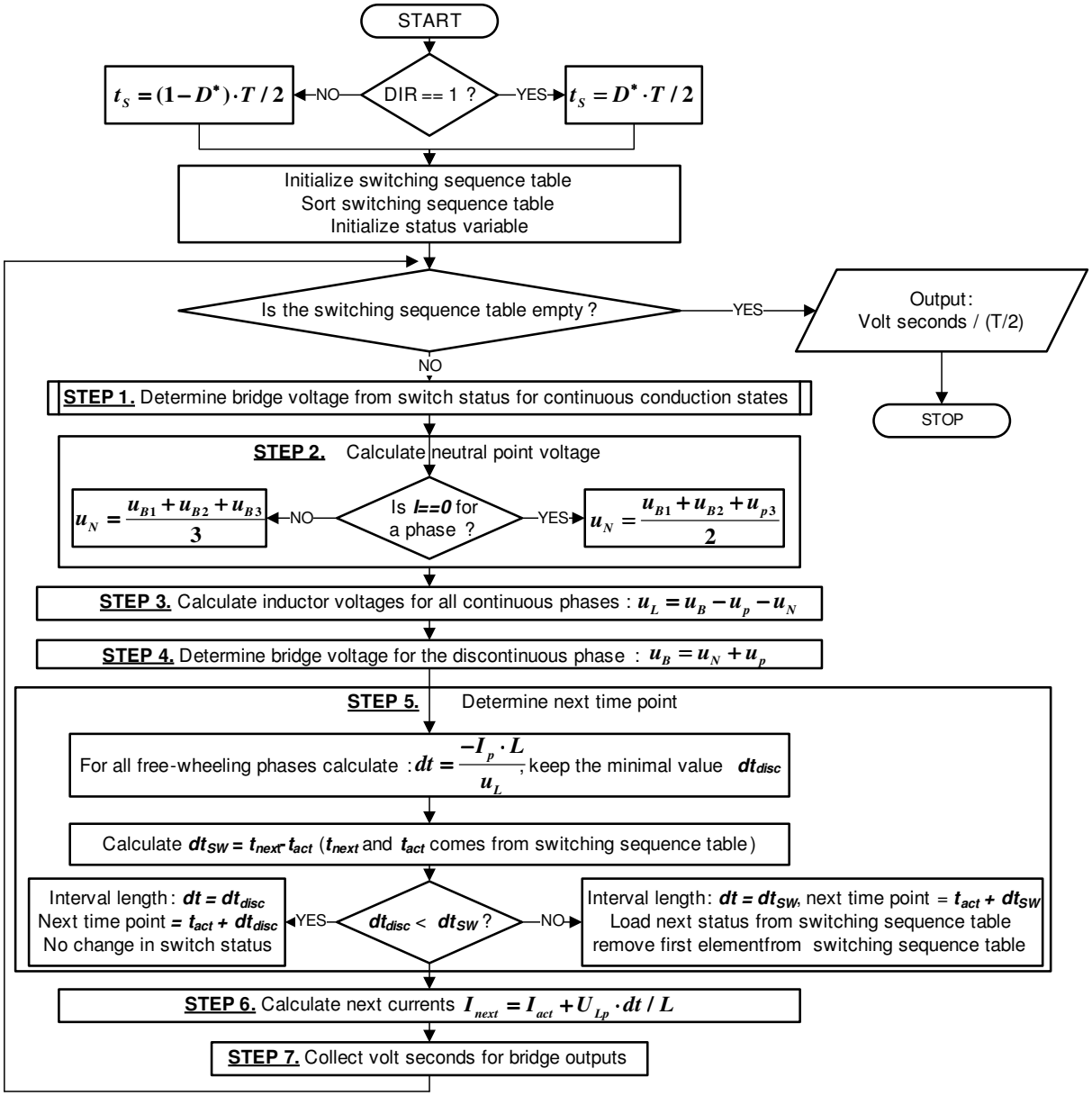


Figure 16. Simplified flowchart of the model used to determine the mean output voltage

Compensation, simulation results

The model described in the previous section requires the following constants: switching frequency, circuit parameters, dc bus voltage, and the value of the effective dead time. The input variables are the phase voltages, the instantaneous phase currents, and the ideal duty ratios (D*) which are the outputs of the current controller, and are valid for a linear (ideal)

inverter. The model is run twice in every switching period: once at the upper corner of the triangular carrier, and once at the lower corner.

The compensator uses the output of the model to calculate a new duty ratio, which - if applied on the inputs of the PWM generator - will result in approximately the same output voltage on the real inverter, as D* would on an ideal one. The bock diagram of this compensator can be seen in Figure 17. It can be seen, that this method can only result in an estimation even if the model is correct, as the method on Figure 17 gives accurate results only for the continuous cases; for discontinuous conduction this is only an approximation. However, as it was shown in section 2.1, the relationship between duty ratio and mean phase leg voltage is a continuous and monotonous function. This shows that multiple iterations of the whole algorithm may improve the results [C5] as shown in Figure 17. The accuracy of the compensation can be increased even further if the actual phase current values can be measured multiple times within a switching period [P1] if actual sampled measurement data can be used instead of the model calculations for some switch states.

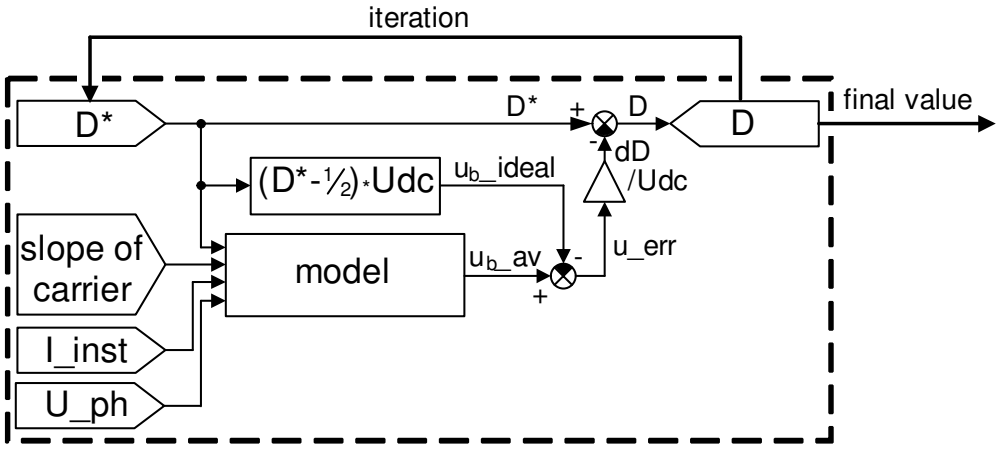


Figure 17. Block diagram of model based dead time compensator

The operation of the method has been tested via simulations in Matlab Simulink. Parameters of the simulated inverter: 400V 50Hz grid connected operation, DQ current vector control, symmetrical / space vector modulation on 8kHz triangular carrier, 3µs effective dead time, filter inductor calculated for 5% of the nominal load impedance at 50A nominal phase current.

The results of the simulation for various loads can be seen in figure Figure 18. The THD values were interpreted for the first 40 harmonics of one phase current. It is visible that the

model based compensator has a significant effect at low currents even if the model is run only once. Running the model multiple times further improves the THD.

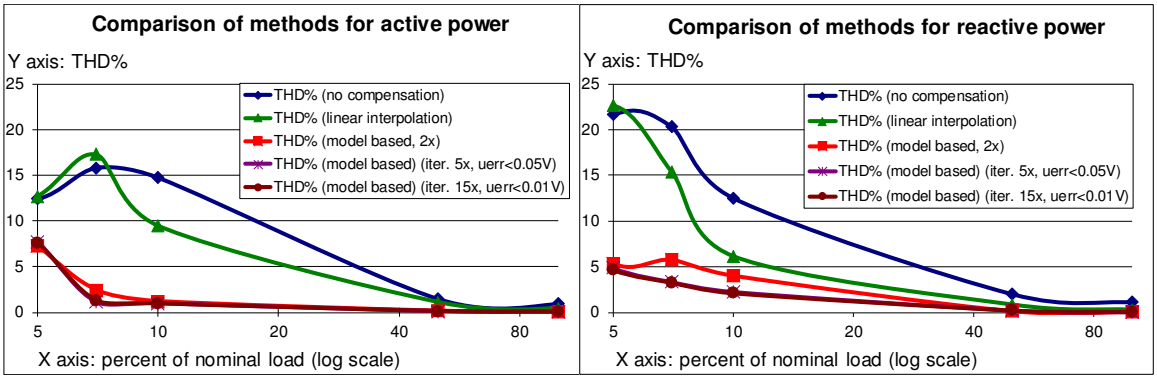


Figure 18. Simulated phase current THD values using model based dead time compensator. Left: for active power, Right: for reactive power

New scientific result – Sub thesis 1.2

Based on theoretical analysis and simulations, the following can be stated as sub thesis 1.2:

I have defined a model based method for estimating the expectable error of phase leg output voltages in the next switching period of three phase two level VSI. The new method calculates with all switching states within a period. I have shown that this model can be used to achieve more accurate dead time compensation than with using the linear interpolation based method. I have shown that repeated execution of the model increases accuracy.

Publications related to thesis group 1: [C1] - [C5], [J1], [P1]

3. High speed simulation of discontinuous conduction

As seen in section 2, a large number of simulations have been performed to demonstrate the usability of the methods described in thesis group 1. As the first thesis group was focused on discontinuous conduction mode (DCM), a simulator was required which is capable of reproducing such behavior without significant slowdown. Simulation of the power circuit of an inverter could be performed using a SPICE-based software, but as most simulations had to be run for some fundamental periods to get usable THD data, this was found to be very slow and the complicated models were hard to set up. MATLAB-based Simscape Power Systems was found to be faster as it uses simpler semiconductor models, but it still calculates with too many variables and the frequent changes in power circuit structure reduce speed. As such, the need has arisen to develop a switching transistor model which is capable of simulating discontinuous conduction, but otherwise is as close to an ideal switch as possible [J2][P2].

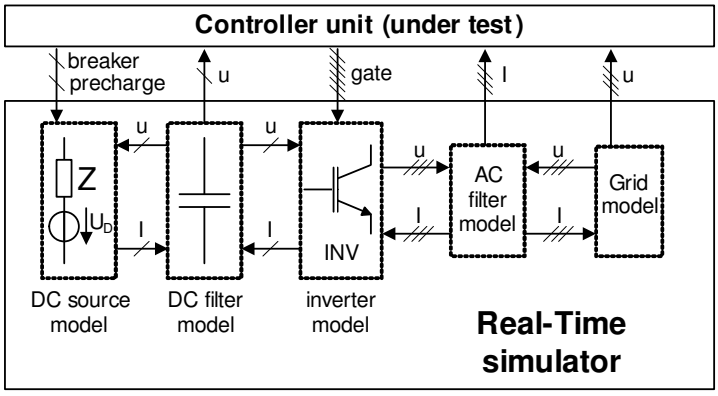


Figure 19. Modular HIL simulator block diagram for three phase inverters.
The arrows show the direction of the data exchange.

Such a fast model can also be beneficial for use in fast real-time simulators. Simulators are advantageous during development, as testing the DSP- or FPGA based control unit of a power converter on the original power circuit is often expensive and dangerous [23][24]. Hardware-In-the-Loop (HIL) simulations can be used instead [25]. The main concept behind HIL simulation is that the high-power parts of the system can be replaced by real-time computational models. Such models can be developed for the power converters [26] and all of the interfacing power and analog measurement components on both sides of the converter, as shown in Figure 19. For example, in the case of an inverter, the components on both the DC side [27] - [29] and the AC side (motor [30] or filter and grid model) can be simulated. The simulator hardware can be connected to the control board under development via real physical

interfaces (analog and digital I/O). As a result, the control card and its software are unable to distinguish the simulator from a real system. Such a simulator can shorten development time and reduce costs [J4]. The hardware used as a real-time simulator may consist of microprocessor or DSP cores. This is useful for the Hardware-in-the-Loop (HIL) simulation of slow [31] or very large systems [32]. However, high resolution real-time simulation is computationally very demanding. FPGA circuits are the core units of very complex [33] and fast HIL simulators [34][35]. Modern FPGAs provide high speed interfaces, low latency and smaller time steps than microprocessors thanks to their paralleled structure [36]. As a result, large FPGAs are usually a better choice for the HIL simulators of power converters than DSPs or personal computers [30][37]. The simplicity of the models is still very important to be able to simulate with low latency and simulation time step.

3.1. Modeling of phase legs

The main building block of most power converters is the phase leg, as shown in Figure 20 for a two-level grid connected inverter. Building a fast and capable model for it is very important for inverter simulation. A phase leg consists of a pair of diodes clamping the switched point of the phase leg (marked as U_{LEG} in Figure 20) to a DC bus, along with controlled semiconductor switches capable of connecting the switched point to certain fixed potentials, e.g. +Udc/2 and -Udc/2 for a two-level inverter. To filter switching frequency voltage components, its load needs to be inductive. This is usually performed in grid connected inverters by the addition of an LC filter.

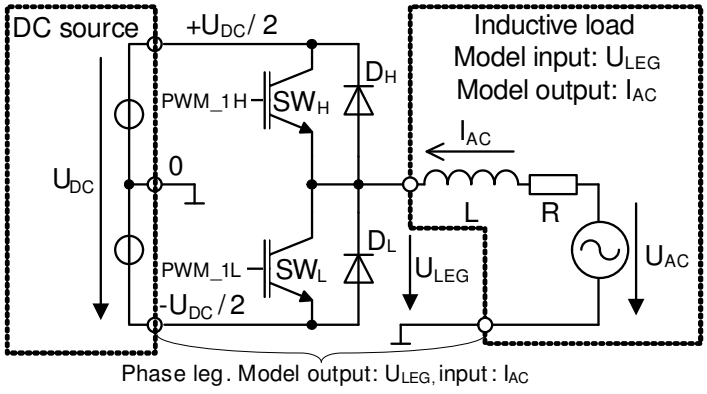


Figure 20. Schematic of a two-level phase leg with inductive load.

A large number of very precise power semiconductor models exist for the described phase leg and its components. Some of them concentrate on the voltage-current characteristics and switching behavior of power semiconductors [38][39]. Others try to implement idealized or identified characteristics [40] or to use parameter extraction and detailed physics based semiconductor models [41][42]. Such models can be very accurate but are highly complicated and computationally intensive, as they use a large number of parameters and solve complicated formulae during operation. They can hardly be optimized for real-time use. The fastest real-time simulators usually need simpler models using a forward Euler solver.

Switching function based models

The simplest solution for modeling semiconductors is probably the switching function model. This is often used in real-time simulators, and sometimes in offline simulators [45]. Figure 21 shows that such a model works by choosing one of the possible voltage levels in each time step. If the high side control is high, the positive voltage is forced to U_{LEG}. If the low side control is high, the negative voltage is forced. If both control signals are low, the sign of the forced voltage is chosen based on the direction of the current. The voltage drop of the semiconductors may also be integrated into the model as shown in Figure 21. Such models can be very fast. However, they cannot handle discontinuous conduction mode (DCM) [34].

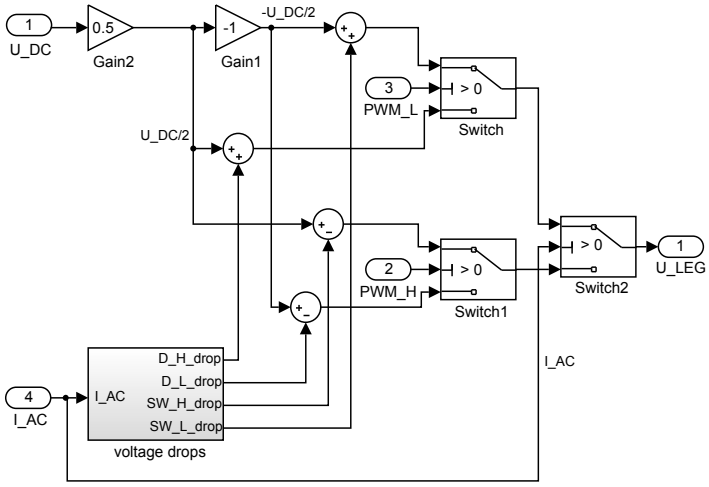


Figure 21. Switching function based MATLAB - Simulink model of a two-level phase leg with inductive load.

In a phase leg working in a PWM converter, there are two situations when both of the switch control signals can be low. One is in an uncontrolled state when the appliance is in the standby or inoperative mode, and the second is during control dead time (introduced to avoid short circuit caused by a delay of the semiconductor switches). In the latter case, DCM

happens only if the current was low before turning off the control, as already discussed in section 2 for thesis 1.

In switching function models, if both of the transistors are OFF in a phase leg, the simple diode model chooses its output voltage for the actual time step based on the polarity of the current. This is done by the "Switch2" block shown in Figure 21. If the control signals remain inactive for a long enough time, the current may fall to zero. This causes the output voltage to alternate between the positive and the negative DC rails, as this type of model only handles continuous conduction and assumes that one of the two diodes is always conducting. In a variable-step solver, simulating DCM with a switching function model causes the time step to decrease to its minimum setting. This results in a serious slowdown of the simulation, rendering the solution impractical with variable-step solvers. The problem may be mitigated using extra logic and communication links between the modules (see Figure 19) to handle the zero crossings, but this degrades the reusability of the modules. Matlab/Simulink has some tools to handle this problem to some extent (e.g. the state ports of integrators cooperating with hit crossing blocks), but these can only be used in off-line simulations.

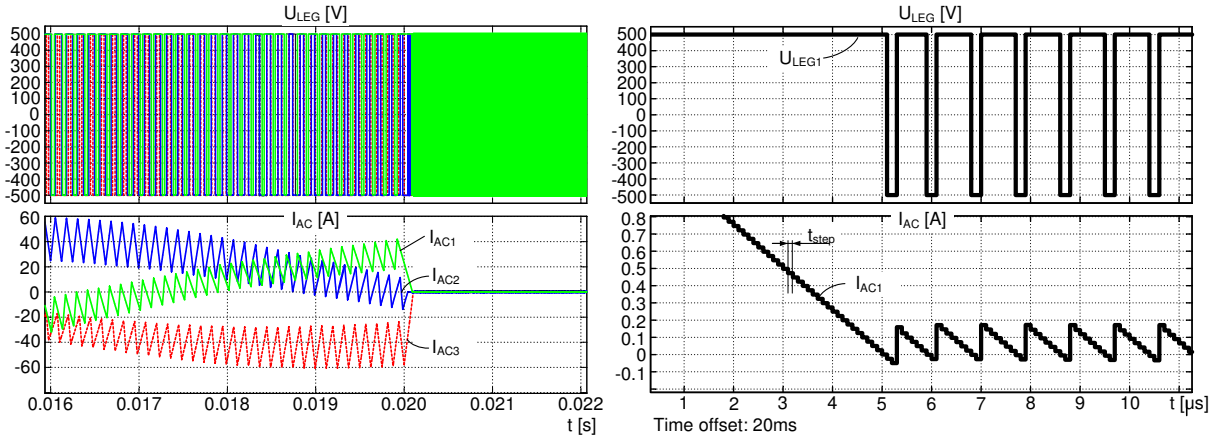


Figure 22. 3-phase inverter waveforms from a switching function based fixed step model. Switch-off and transition to DCM is magnified for phase leg 1 (right).

Fixed step solvers do not suffer from such problems, but the simulation of phase leg voltage and current values during DCM is still problematic. A switching function model operating in DCM on a fixed step solver generates a false high frequency pulse train on the phase leg voltage waveform, which has a period proportional to the time step. Such waveforms can be seen in Figure 22. The minimal pulse width of this high frequency noise is one simulation time step.

The switching operation causes small ripples in the inductor current, which are visible on the right side waveform of Figure 22. The average of the simulated phase leg voltage, seen in the diagram, is still correct, equal to u_{AC} (Figure 20).

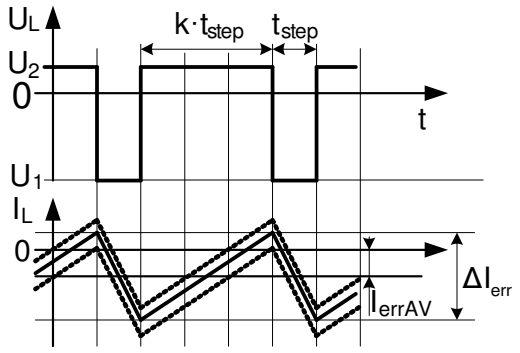


Figure 23. Inductor voltage and current waveforms of a switching function based model during DCM

There are problems with common mode currents and energy balance as well, as a result of the simulation error described above. A small triangular current always flows through the simulated inductively loaded phase leg during the DCM. The typical inductor voltage and phase leg current waveforms caused by this can be seen in Figure 23. In the equations below, U_1 and U_2 represent the two possible voltage values of the filter inductor L based on the polarity of the current, in the following order:

$$|U_1| > |U_2| \tag{2-1}$$

The resulting ripple of the falsely simulated error current can be calculated as follows:

$$\Delta I_{err} = \frac{|U_1| \cdot t_{step}}{L} = \frac{|U_2| \cdot k \cdot t_{step}}{L} \tag{2-2}$$

Equation (2-2) enables the calculation of both the time ratio k in (2-3) and the noise frequency f_{err} in (2-4). k is a whole number. Thus, it needs to be rounded upwards, as shown by the operator $\lceil\ \rceil$ in (2-3):

$$k = \left\lceil \frac{|U_1|}{|U_2|} \right\rceil \tag{2-3}$$

$$f_{err} = \frac{1}{(1+k) \cdot t_{step}} \tag{2-4}$$

Based on Figure 23 and (2-3), it is clear that the average simulated inductor current is nonzero if the two possible inductor voltages are different $U_1 \neq U_2$. The actual offset of the current

may vary between periods, since the actual zero crossing might happen anywhere up to one time step before the simulator recognizes the change in the polarity of the current. Therefore, the offset of the triangular current can change between its minimum and maximum value, as shown with the dotted lines in Figure 23. The average error current can be calculated as follows:

$$\left|I_{errAV}\right| = \frac{\Delta I_{err}}{2} - \frac{\left|U_2\right| \cdot t_{step}}{2 \cdot L} = \frac{\left(\left|U_1\right| - \left|U_2\right|\right) \cdot t_{step}}{2 \cdot L} \tag{2-5}$$

The problem is that the false square wave phase leg voltage and current ripple makes it hard to test certain protection hardware and software. This includes hardware based dead time compensators using phase leg voltage measurement, back EMF measurement during the DCM (e.g. sensorless BLDC drives), and leakage current protection (e.g. electric car chargers). A major problem is that if a DC capacitor model is attached to the phase leg model, the rectified false current ripple constantly charges the input capacitor. The resulting error becomes significant if the control of the phase leg is disabled for several milliseconds. This can falsely trigger DC overvoltage protection.

Simulation of junction capacitance

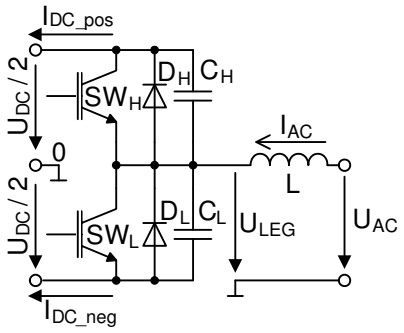


Figure 24. Modeled capacitances of a phase leg.

Adding a junction capacitor model, as shown in Figure 24, can provide an acceptable phase leg voltage when simulated in place of the open switch [43]. For AC currents, the DC grid can be substituted with a short circuit. Thus, only one capacitor model is required for each leg. A saturated integrator can be used instead of the switch-based model, and the gate signals and current direction can be used to determine the saturation limits. If none of the switching transistors is controlled, the maximum and minimum saturation values need to be set to the positive and negative DC bus voltages. The integrator used in the test phase leg model was used to simulate the diode leg operation only. It was forced to store the forced phase leg

voltage value if any of the semiconductors is conducting. Figure 25 shows the actual model built in MATLAB Simulink. The capacitance was modeled as an integrator with external reset, external saturation values, and external initial condition. The high and low saturation limits were modified based on the control signals. The integrator was forced to RESET if any of the two IGBTs were controlled (external reset input in Figure 25) or if any of the two diodes were conducting. This latter condition was detected by the logic of Figure 25: if the saturation is working and the current is flowing in such a direction that it maintains the saturation, then the model assumes diode conduction. During the reset, the value in the integrator modeling the junction capacitance was selected to be the phase leg voltage (as forced by the semiconductors).

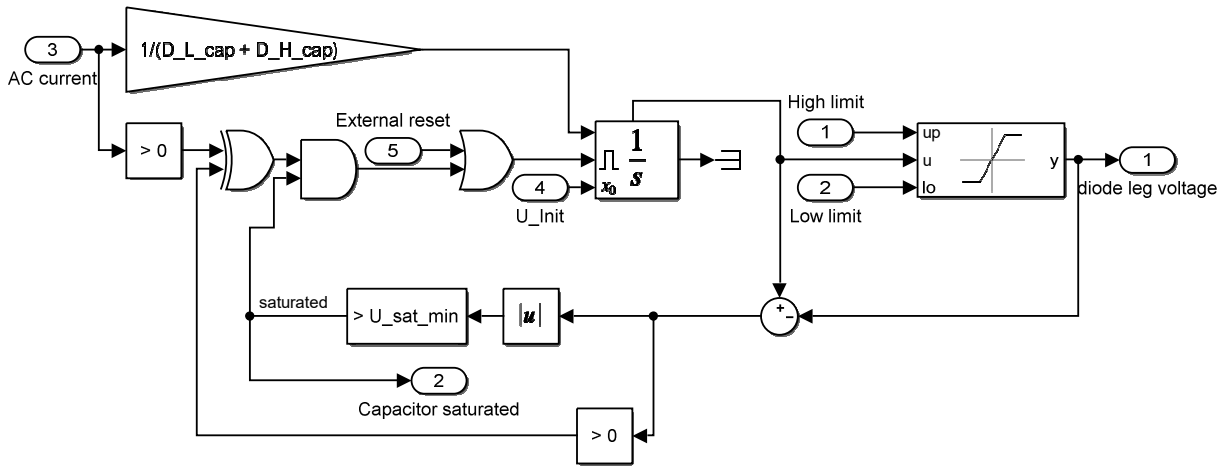


Figure 25. Matlab Simulink block diagram of the junction capacitor based phase leg model.

Using the capacitor model, the DC currents on both the positive and negative DC rails can be easily calculated:

$$I_{DC\_pos} = I_{AC} \cdot \frac{1}{1+\frac{C_L}{C_H}} \tag{2-6}$$

$$I_{DC\_neg} = I_{AC} \cdot \frac{1}{1+\frac{C_H}{C_L}} \tag{2-7}$$

When used with the saturated integrator model, the formulae (2-6) and (2-7) described above can solve the DC current offset problem shown in (2-2).

The operation of the model can be followed based on the example of a three phase grid connected inverter (Figure 26). After disabling the gate signals, a decaying high frequency oscillation appears on each of the phase legs superimposed onto the fundamental AC voltage. The frequency is so high that individual periods cannot be seen in Figure 26. However, the resulting waveforms are realistic and enable the testing of protection and control units.

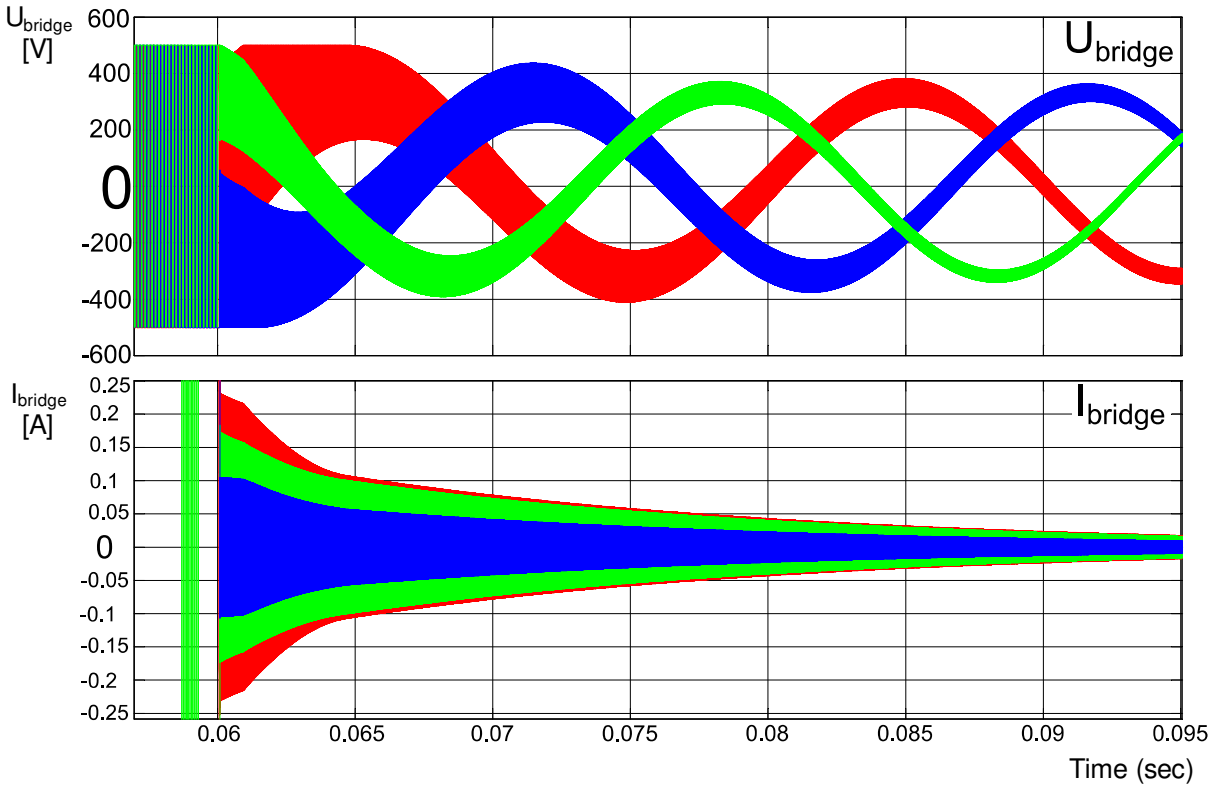


Figure 26. Junction capacitor modeling example: voltage and current waveforms of a three phase inverter after disabling the gate signals.

In theory, the capacitor model can also be used to estimate the switching losses of the bridge. This can be done by subtracting the lost energy from the value of the integrator in the DC capacitor model.

The time step required for simulation of the true junction capacitance present in the actual semiconductors is usually very small. If the capacitance is in the 100pF to some nF range, and the connected inductor is in the 100µH to 1mH range, the resulting resonant frequency can reach several MHz. If the forward Euler solver is used, this would necessitate time steps of much less than 100ns to avoid positive feedback and instability of the model. This increases the processing power required to run the simulation which in turn lengthens simulation time. The required time step is usually so small that real-time simulation of such models is not feasible even with FPGA-based simulators. Using too long simulation time steps can lead to

stability problems, which necessitates the use of a backward Euler solver and further simplifications such as the associated discrete circuit (ADC) model [44]. However, this method may still be useful in certain offline models.

The required computing power can be decreased if the simulated junction capacitance is increased to be orders of magnitude larger than the true value. This results in unrealistic simulation results with low frequency decaying oscillations. However, this may be sufficient in several cases and can speed up the simulation considerably.

Structure changing or state machine based phase leg modeling

To avoid the problems described before with junction capacitance simulation, it seems to be a good idea to develop a model which modifies the load model in zero current state instead of treating the problem in the phase leg model. It is indeed possible to make a simple logic function that, in case both switches are open and the current is approximately zero, forces the leg voltage to be equal to the back EMF voltage (which is in our case the grid voltage) and freezes the integrator modeling the inductor. In case of simple power circuits, such a model requires less computation, and it runs fast in off-line simulation.

However, such models can quickly get very complicated for higher order loads containing multiple inductors or capacitors. In case of an inductor, if the current is reduced to zero, such a model can change its state and substitute the inductor with an open circuit. This works fine so far, but in such a model we need to find and set all possible trigger conditions, under which conditions the open circuit needs to be removed and the integrator needs to be restarted. This is simple for one inductor but becomes impractical for polyphase circuits or for circuits containing models of transformers modeled with stray and magnetizing inductances. In such cases, the large number of inductors and voltages can make the trigger conditions very complicated. Such a model will not be modular because the trigger condition will be tied to the power circuit being modeled. So contrary to the ideas shown in Figure 19, any modification on the power circuit would require the re-evaluation and modification of the trigger conditions. A more universally useful model would have several advantages over the structure changing or state machine based model. I conducted further research in this direction.

3.2. Proposed PI controller based phase leg model

In order to develop a fast model, the switching function based model of Figure 21 was used as a basis. This model does not contain additional state variables apart from the filter components of the power circuit, and it can be simulated using a small simulation time step and a low latency. In order to be able to use the model in an FPGA-based simulator, the ordinary differential equations (ODE-s) of the dynamic components need to be solved in real-time, which is easy to do on simpler models with a fixed-step solver like the Forward Euler method. More complex methods such as a backward Euler or a Runge-Kutta solver mean a much higher computational burden for the FPGA [46]. The Forward Euler method has accuracy and stability problems when simulating second order oscillating elements [47][48]. This was a problem in the case of the junction capacitor-filter inductor circuit described in the previous section and shown in Figure 24, since the period of the high frequency oscillation may be shorter or not much longer than the time step. Very accurate real-time simulation of these oscillations is practically hard, since the value of the capacitances are not constant, and often not accurately known. However, accurate simulation of this is usually not needed. In real appliances, such oscillation frequencies are generally so high that these are instantly filtered by a passive RC anti aliasing and noise filter. Such a filter is usually present anyway on the analog input stage of the controller. As a result, direct junction capacitor modeling is rarely used in longer or real-time simulations apart from special applications like ZVS resonant bridges [49], where large external capacitances are paralleled to semiconductors. In other cases, an approximation of the DC and low frequency components of the phase leg voltage are usually sufficient if the phase leg is not controlled and the current becomes discontinuous.

In order to solve the problems of the switching function based model, a moving averaging stage can be added after the current and phase leg voltage outputs of the model. This gives the correct phase leg voltage. However, it also increases the delay of both the voltage and current signals, and it is unable to remove the DC component of the current. Another method is described in [50] using a resistor divider. This models IGBTs correctly. However, it needs an iterative algorithm for diode simulation.

The proposed method uses a discrete-time PI controller. The structure of the bridge model can be seen in Figure 27. When both of the switches are off and the current has decreased to zero, the PI controller automatically finds the correct phase leg voltage in each of the time steps required to keep the current at zero.

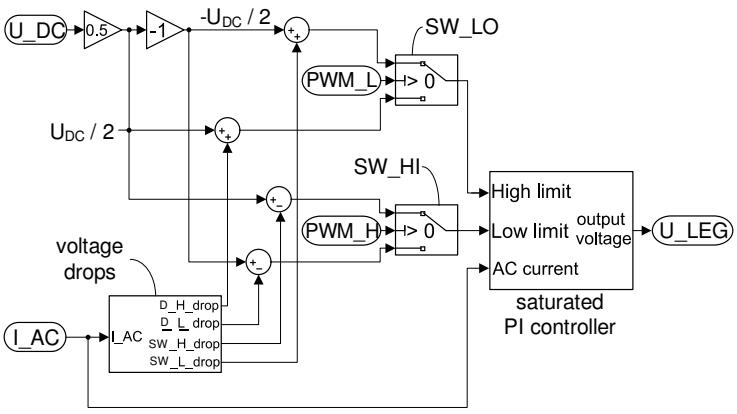


Figure 27. Phase leg model structure using a saturated PI controller.

The calculated phase leg voltage follows the voltage of the grid or the motor back EMF as long as the PI controller is not saturated. The output saturation limits are set to the full DC bus voltage range if both of the switches are off. The voltage drops of the diodes can also be added to this model, as shown in Figure 27. If the control signal of a switch becomes high, the saturation limits are modified so that the output voltage remains in the range allowed by the corresponding switch and diodes. This operation may also be extended to multilevel converters by correctly choosing the low and high limits from the possible values based on the actual state of the switching semiconductors.

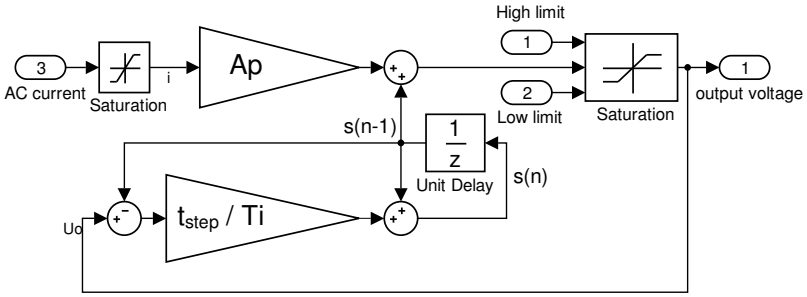


Figure 28. Structure of the saturated PI controller used in the phase leg model of Figure 27.

The structure of the actual PI controller configuration can be seen in Figure 28. t_{step} is the simulation time step of the discrete time model, *Ap* is the proportional amplification and *Ti* is the integration time constant of the PI controller. The implementation of the saturation in the PI controller uses the so called automatic reset or Foxboro anti-windup scheme [51] [52],

which is simple and easy to implement. In this implementation, the integral action is implemented by applying positive feedback with a first-order low-pass filter. If there is no saturation, the integrator integrates the error (in this case the AC current) multiplied with $A_p \cdot t_{step}/T_i$ and as such it is mathematically equivalent to an ideal PI controller. The implementation seen in Figure 28 was chosen to avoid the oscillations arising from rapid current changes in the continuous conduction mode.

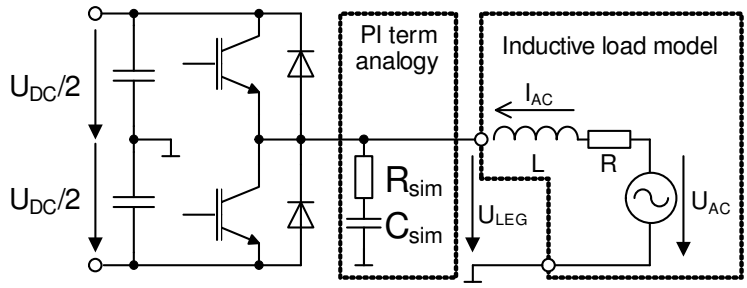


Figure 29. Circuit emulated by the PI structure of Figure 28.

This realization imitates the behavior of a series RC element similar to that of the circuit shown in Figure 29. The described PI structure is actually mathematically identical: R_{sim} can be substituted for *Ap* and $R_{sim} \cdot C_{sim}$ can be substituted for the time constant *Ti* in Figure 28 when there is no semiconductor conduction. The saturation is placed directly onto the output of the PI controller, which is equivalent to the phase leg voltage. The input value of the integrator resembles the input current of the capacitor, and it is proportional to the difference between the integrator value and the actual (saturated) output voltage.

To tune the PI controller, some information is required on the rest of the power circuit. This information includes the approximate inductance value during the DCM (L_{disc}), the DC voltage and the simulation response time (i.e. the control system dead time). Since two parameters are required, the inverter model cannot be completely independent from the load model as described in Figure 29. However, these parameters are not required to be accurate (the high frequency oscillations of the junction capacitance voltages cannot be accurately simulated with long time steps anyway). The only goal is to keep the system stable. The value of L_{disc} is the approximate net inductance seen by the AC side of the converter. Iron core saturation does not need to be included in the calculation, since the PI controller only operates at nearly zero currents. Too high of an L_{disc} value might cause divergent operation, and too small a values might lead to oscillations. The simulation response time (t_{SIM_RESP}) needs to be equal to $t_{step}/2$ (the average delay caused by the integrator in the PI controller) plus any other delay present in the controlled circuit. The formulas for calculating the PI controller

parameters can be seen in (2-8) - (2-12). The tuning described below is for maximum disturbance rejection. However, other methods (e.g. Ziegler-Nichols) may be used with success. The calculation leaves a pre-defined phase margin φ_{margin} and uses up the remaining phase shift by leaving 2/3 of it for the dead time component and 1/3 for the integrator:

$$\varphi_0 = \frac{\pi}{2} - \varphi_{\text{margin}} \tag{2-8}$$

$$\omega_c = \frac{2}{3} \cdot \frac{\varphi_0}{t_{\text{SIM\_RESP}}} \tag{2-9}$$

$$T_i = \frac{1}{\omega_c \cdot \tan\left(\frac{1}{3}\varphi_0\right)} \tag{2-10}$$

The A_p parameter was calculated so that the absolute open loop transfer of the current loop is 1 at ω_C frequency:

$$A_p = \omega_c \cdot L_{\text{disc}} \tag{2-11}$$

It can be seen that Figure 28 contains a saturation block directly on the input of the PI controller. The I_{lim} value is defined as:

$$I_{\text{lim}} = \frac{U_{\text{DC}}}{A_p} \tag{2-12}$$

I_{lim} is used to limit the input current of the PI controller so that it can cause no more than a U_{DC} voltage difference in the next time step. This can be allowed since any input current higher than I_{lim} has the same effect anyway because of output saturation. The advantage of this is that it can help to avoid loss of precision in floating point simulators, or it can reduce the number of bits required and avoid overflow when used in a fixed-point model.

Simulation results for switch-off and discontinuous conduction

The new PI controller based model has been tested on a three phase grid connected inverter by disabling the gate signals. This lets the phase currents decrease to zero. The resulting Simulated waveforms shown in Figure 30 are directly comparable to those of Figure 22. The phase currents are controlled to zero very quickly, which means that the simulated DC current will also be zero. The high frequency oscillations caused by the junction capacitances are not simulated, but the phase leg voltages stabilize at the voltage of the output capacitor.

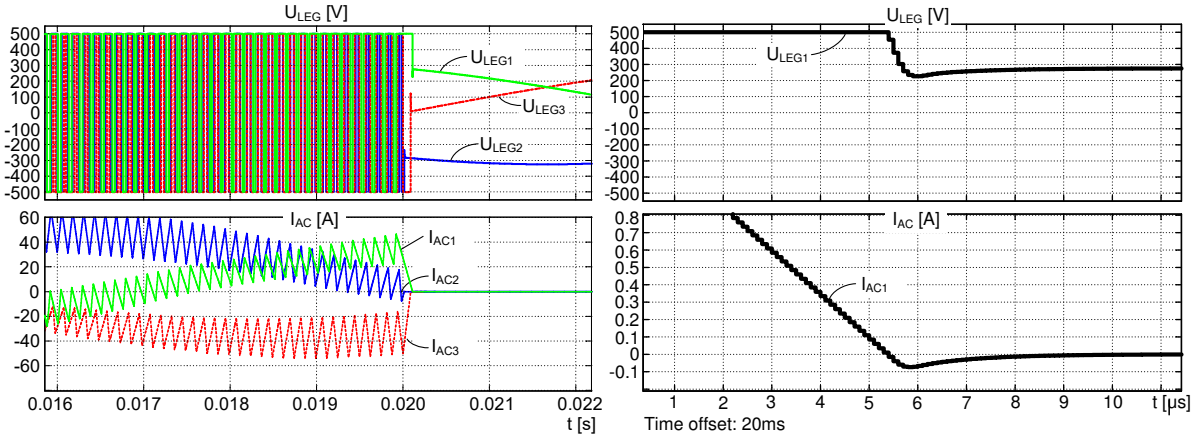


Figure 30. 3-phase inverter waveforms from the new PI controller based fixed step model. Switch-off and transition to DCM is magnified for phase leg 1 (right).

The new PI controller based phase leg models have also been tested for discontinuous conduction during dead time. As a comparison, the simulations were also performed with switching function based phase leg model. The power circuit was also built in Matlab Simscape Electrical, this model is visible in Figure 31. This Simscape Electrical model uses an RC snubber between the collector and emitter pins of each IGBT, so basically it can be understood as a junction capacitance based model.

For this junction capacitance model, the R and C values were set to 250pF and 0.1Ω per IGBT. For the switching function and the PI controller model, the time step for the inverter model was t_{step}=50ns. In all three simulations, switch control signals with a switching frequency of 8kHz and a relatively large effective dead time of 5µs were used. The simulated inverter was working from 1000V DC onto a 3 phase 400V grid through an inductance of 450 µH and a resistance of 2.5mΩ.

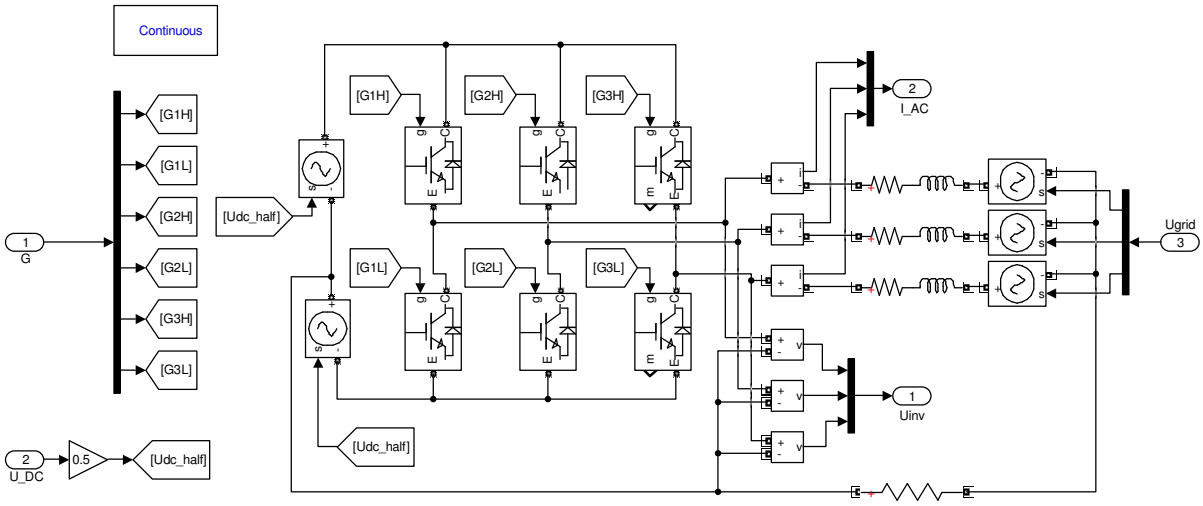
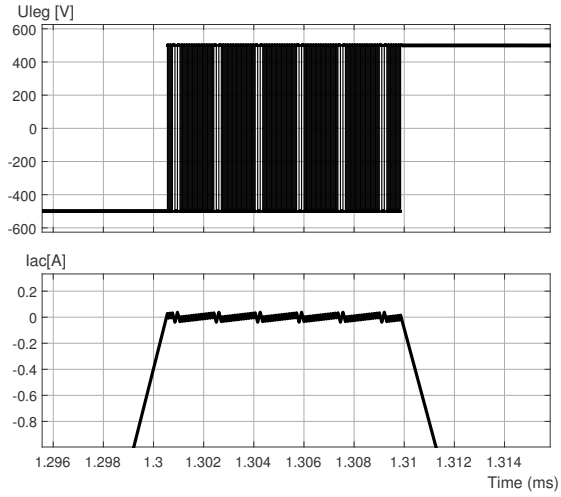
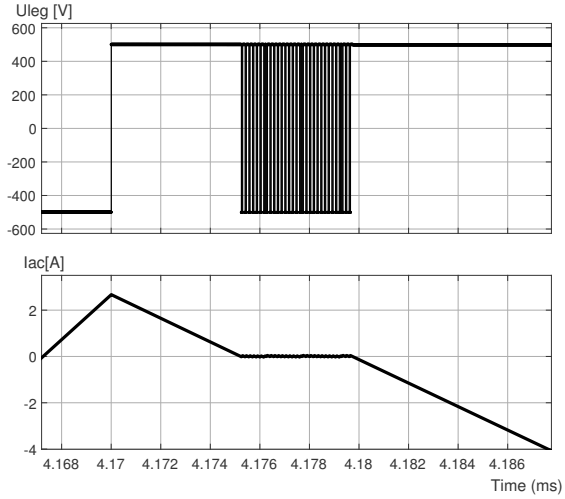


Figure 31. Three phase inverter modeled using MATLAB Simscape Electrical. This environment models each IGBT-diode pair with a series RC snubber when not conducting.

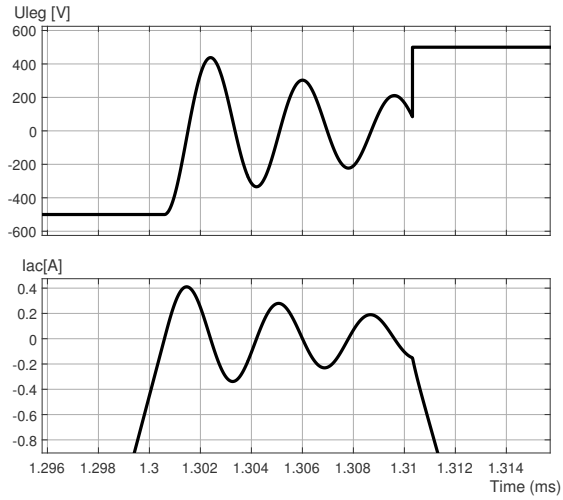
Simulation results obtained for discontinuous conduction during dead time with these three models (switching function based, junction capacitance based, PI controller based) are shown in Figure 32 under identical circumstances. The discontinuous cases described in Figure 8 of section 2 for thesis 1 are recognizable on the simulations in Figure 32. The switching function model switches at high frequency between the two DC voltages during discontinuous conduction and the subharmonic oscillation is also recognizable to some extent. Using the junction capacitance model results in a decaying oscillation around the grid voltage during discontinuous conduction. This is the closest to actual reality but its computational requirements are more substantional, especially for low power inverters with small value junction capacitance and filter inductors. The PI controller based model works as expected: it finds the value of the grid voltage in about 15 time steps in both cases. The oscillation is missing, but the mean values are the same as with the junction capacitor modeling. The actual results show some overshoot caused by the PI controller, but this can be further reduced by slowing down the controller via increasing the phase margin or decreasing the duration of the time step $t_{step.}$



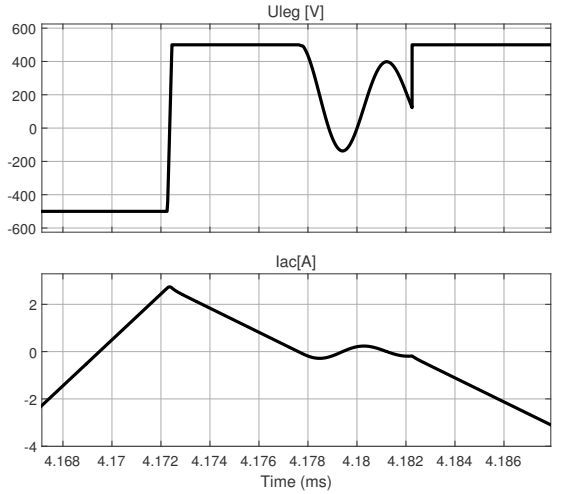
a2 waveform on switching function model



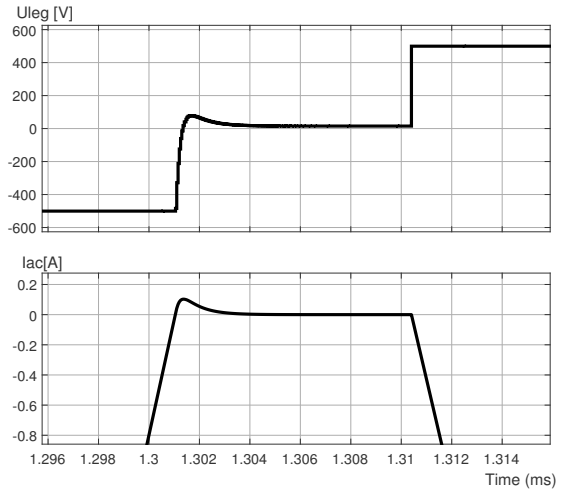
a1 waveform on switching function model



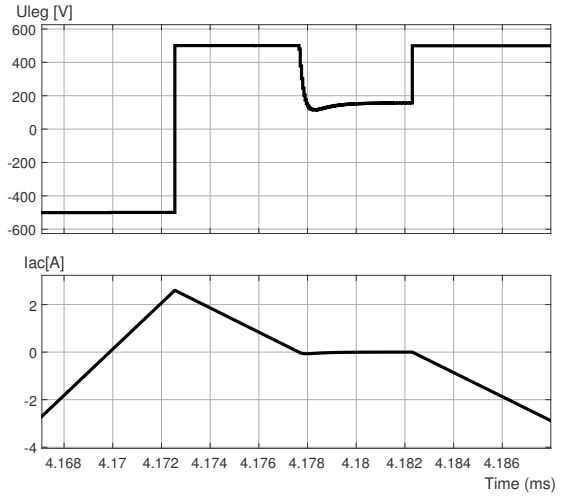
a2 waveform on junction capacitance model



a1 waveform on junction capacitance model



a2 waveform on PI controller model



a1 waveform on PI controller model

Figure 32. Simulation of cases of discontinuous conduction previously discussed in Figure 8 using PI controller, junction capacitance, and switching function based models.
The top diagrams show the voltage, and bottom diagrams show the current of one phase leg.

3.3. New scientific result – Thesis 2:

Based on theoretical analysis and simulations, the following can be stated as thesis 2:

I have shown that the output voltage of the switch based phase leg model shows a limit cycle operation during control dead time and then the phase leg is off. I have shown that by including the junction capacitance in the model, discontinuous conduction can already be simulated. I have made a fast phase leg model based on a discrete PI controller. I have shown that the model can approximate well the voltage of the switched point, and that it can be used for the simulation of discontinuous conduction during dead time.

Publications related to thesis group 1: [P2] [J2]

4. Harmonic Emissions caused by Flat-Top Modulation

General three-phase sinusoidal PWM modulated voltage-source inverters (VSI) such as the one already shown in Figure 11 and in Figure 35 allow the arbitrary choice of the zero-sequence duty ratio component. This is allowed as usually there is a very high zero sequence (also called common mode) impedance between the DC bus (input) and the AC bus (output) of an inverter, and no significant zero sequence current can flow. The grid or motor load only sees the phase-to-phase voltages of the three phase system. The three phase voltages are only limited by the DC bus voltage, allowing the use of various zero sequence modulations for different purposes [56]. To reduce switching losses, the Flat-Top (also called discontinuous PWM 1 or DPWM1, two-phase, or 60° bus-clamp) PWM modulation method is often used in three phase inverters.

The original Flat-Top modulation was first described by Depenbrock [53] under the name DPWM1 and was further investigated by J. W. Kolar [54]. The modulation technique is one of the most widely used three phase modulations in the industry, next to the symmetrical or space vector modulation [55] which can be used to extend the output voltage range while maintaining low current ripple. These modulations, along with other popular waveforms are summarized in [57] and [62]. A correct summary of DPWM0 to DPWM3, DPWMMAX and DPWMMIN can be found in [63].

The main advantage of Flat-Top is a significant improvement in efficiency. In this type of modulation, the zero-sequence duty ratio is chosen in a way that the phase leg with its duty ratio closest to 1 or 0 remains connected to the closest DC rail. This operation can be seen in Figure 33. The result is that each phase leg is switched for only 2/3 of a fundamental period, each phase leg is tied to the positive DC rail for 1/6, and to the negative DC rail for the remaining 1/6 of a fundamental period. The clamped phase leg changes at every 60° electrical angle. The resulting zero sequence signal has 6 steps per period, as shown by the actual waveforms in Figure 34. The advantage of this modulation is that the switching losses are decreased by up to 1/2 for symmetrical active currents in phase with the voltage.

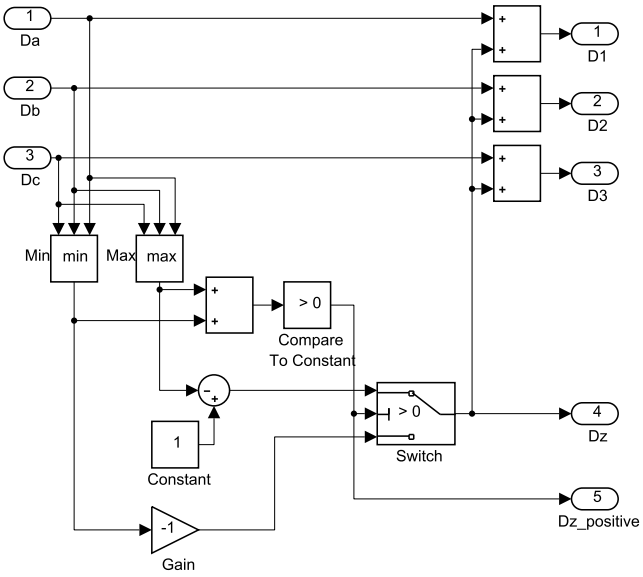


Figure 33. Block diagram of a 60° Flat-Top modulator realized in Matlab Simulink

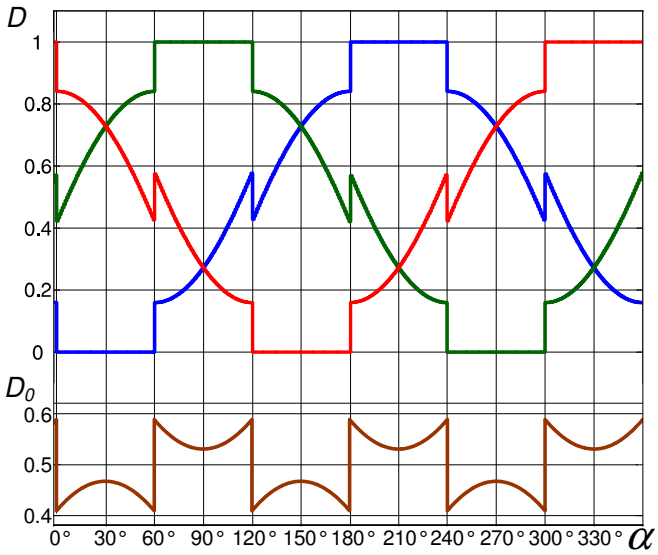


Figure 34. Waveforms of the classical FLAT-TOP modulation. Top figure: duty ratios of the top transistors of the phase legs. Bottom figure: zero sequence component.

The Flat-Top modulation method has been generalized to improve efficiency for reactive currents and unbalanced loads as well [59]. Similar schemes have been investigated for other topologies as well. A five-phase version of all six DPWM methods has been analyzed in [64], and the usage of DPWM methods for more than five phases is investigated in [65]. Vienna rectifiers can take advantage of the original 60° Flat-Top (DPWM1) waveforms as well [66] [10]. Three-level NPC-type inverters can use similar discontinuous PWM methods to achieve lower current ripple and increased efficiency as described in [60], [58], and [67] - [70].

DPWM methods have also been considered with the goal of loss reduction in parallel interleaved converters [71], modular multilevel converters [72], cascaded H-bridge converters [73] and back-to-back converters [74], although the issue of increased current ripple on inductors and capacitors is problematic in certain applications. Compared to traditional CBSM (Carrier Based Subharmonic Modulation), current ripple and - in case of drives - torque pulsation is increased with all discontinuous PWM methods to a varying degree. The DPWM3 method is analyzed from this point of view in [75].

In the following discussions, the described phenomena are easier to understand based on the the actual carrier, duty ratio, and current waveforms. In the following sections the calculations will be applied using line voltages (u_{C12}, u_{C23}, u_{C13}) and currents (i_{12}, i_{23}, i_{13}), as shown in Figure 35. Line currents will be interpreted as currents flowing on capacitors and loads connected between phases in delta configuration. The usage of line waveforms described above eliminate the zero-sequence current and voltage components from the equations. The resulting waveforms are easier to understand with CBSM in mind, as opposed to using space vectors which can result in more complex waveforms.

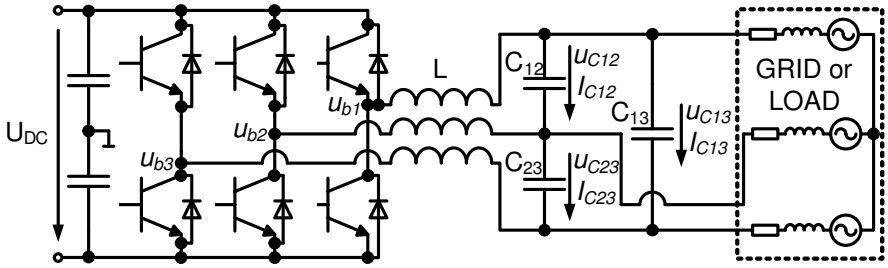


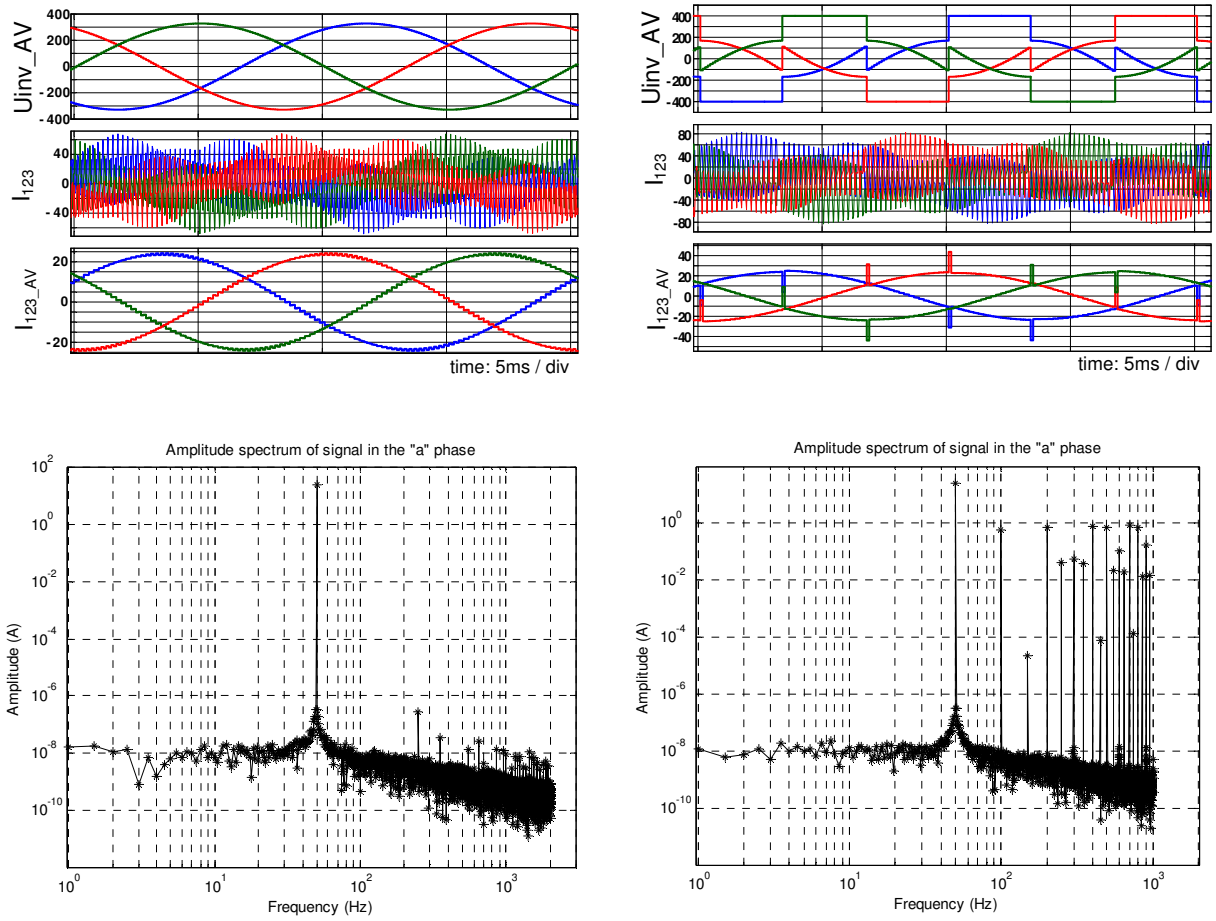
Figure 35. Three phase two-level VSI with low pass filter for grid connected or stand-alone operation, with the filtering capacitors are shown in delta connection.

To simplify the investigation, the circuit configuration shown in Figure 35 was used. It was assumed that the load currents have only fundamental components, and all harmonics of the switching frequency currents flow only through the Δ-connected capacitors C12, C13 and C23. While this is not true in real life circumstances, it is true for a grid forming inverter in no-load conditions, which is easy to test. It can also be assumed that if the inverter is capable of generating sinusoidal voltage waveforms under these circumstances, then its current will also be sinusoidal when connected to the grid, if other nonlinearities and external sources of harmonics are neglected. To further simplify the theoretical analysis, the fundamental frequency current components were omitted from the analysis by assuming the load current to

be constant during a switching period. This can be done, because the LC filter of the inverter can be assumed as a linear system, and the distortion caused by Flat-Top happens 6 times per period, so it is not expected to result in significant fundamental frequency currents.

4.1. Current transients caused by zero sequence steps

Measurements with actual inverters having small filter inductors have shown that significant high current spikes can occur with flat-top modulation in certain operation conditions. These may be sufficiently high to trip overcurrent protection. These high current spikes were not detected on the same inverter, if symmetrical modulation was used instead of the flat-top. Simulations done in Matlab Simulink have also shown similar results, as shown on Figure 36.



a. pure sinusoidal modulation

b. 60° flat-top modulation

Figure 36. Average phase leg voltages (Uinv_AV), actual(I_{123}) and average (I_{123_AV}) phase currents, spectrum of one phase current of a simulated grid connected inverter with RL filter

The waveforms seen on Figure 36 were generated using an ideal inverter model with no semiconductor delays, no voltage drop, and no dead time. The filter capacitors seen in Figure 35 were not included in the model, only an LR element of L_s=200μH and R_s=0.1Ω was simulated between the inverter and the standard 230V 50Hz grid. The simulated inverter was running at a carrier frequency of 5kHz from a 800V DC bus. The inverter was set to produce 232V RMS phase voltage on the inverter-side of the grid (Uinv_AV on Figure 36). Figure 36a shows results without modulation, while Figure 36b shows results using flat-top. The spectra of one of the phase current signals are also shown. The THD of this current signal calculated for the first 40 harmonics was 0.1139 for the flat-top case, and 1.4147×10^{-8} for the sinusoudal modulation. The latter number is very small and can be evaluated as an accumulation of truncation errors. The averaging used for the calculation of U_{inv_AV} and I_{123_AV} graphs of Figure 36 was done using an averaging window of two consecutive half switching periods.

Based on the operation of flat-top modulator, it can be expected that the distortion is higher if a low output voltage is produced from a relatively high DC voltage. With a flat-top modulator, this low modulation depth operation results in high amplitude steps in the zero sequence duty ratio component which can lead to common mode EMI problems [56]. But this alone should not cause problems in the differential output currents.

The current ripple waveforms resulting from the use of Flat-Top modulation have been investigated in [C6] and in [C7]. The time-domain analysis shows that the stepwise waveforms appearing once in every 60° in the zero-sequence component cause a phase shift or a waveform change in the line voltage and current. In [C7] it has been shown that the resulting transitional voltage and current waveforms are not symmetrical to the original average line current, and the integral of a current waveform for the transition period is not the same as for the periods before or after the transition. In case of stand-alone or grid-connected inverters shown in Figure 35, the changes in inductor current waveform cause a transient in the AC side output voltage and current once in every 60°.

Although this type of Flat-Top distortion is relatively minor in most inverters, it may cause problems under certain circumstances. Such are if the inverter uses low value low cost underdamped LC or LCL filter circuits on the AC side with resonant frequencies closer to the switching frequency, if the inverter runs at a modulation index close to 50%, or if the switching frequency is relatively low, close to the fundamental frequency. The distortion was first observed in an active rectifier during grid synchronization, when the AC voltage was

ramped up before closing the grid side AC contactor, causing erroneous voltage amplitude readings and problems in the synchronization state machine.

The cause of the problems can be better understood by investigating the operation of the Flat-Top modulator seen in Figure 33, and by better understanding the operation of a carrier based PWM modulator. A sampled PWM modulator generates a triangular waveform, to which the duty ratios are compared. The controller of the inverter determines the new duty ratio values for each half period. These are set in the PWM modulator at the beginning of the half-period, and then remain unchanged for that half-period. Any change in the zero sequence duty ratio component, including the step signal parts, become effective only from the peaks of the triangular carrier wave.

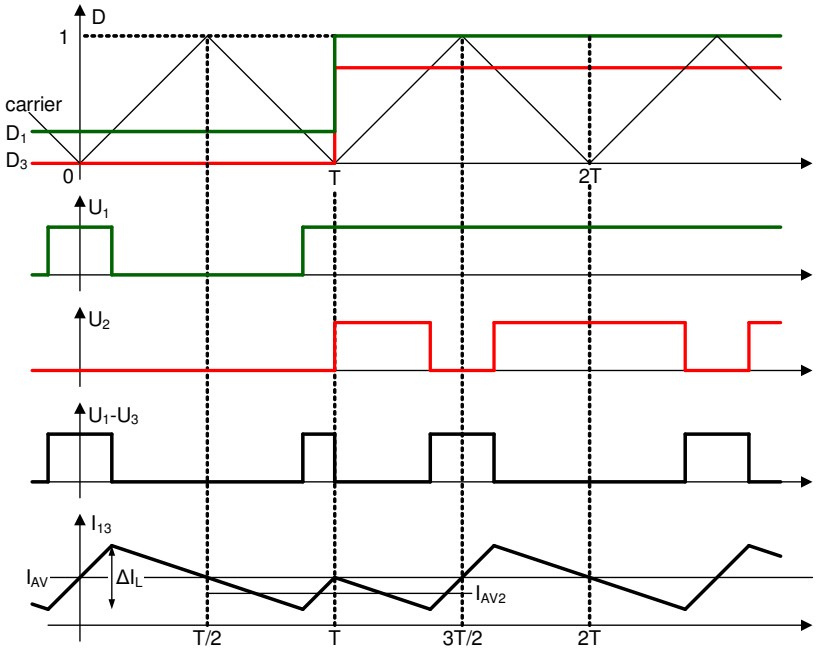


Figure 37. Waveforms for Type 1. zero sequence step

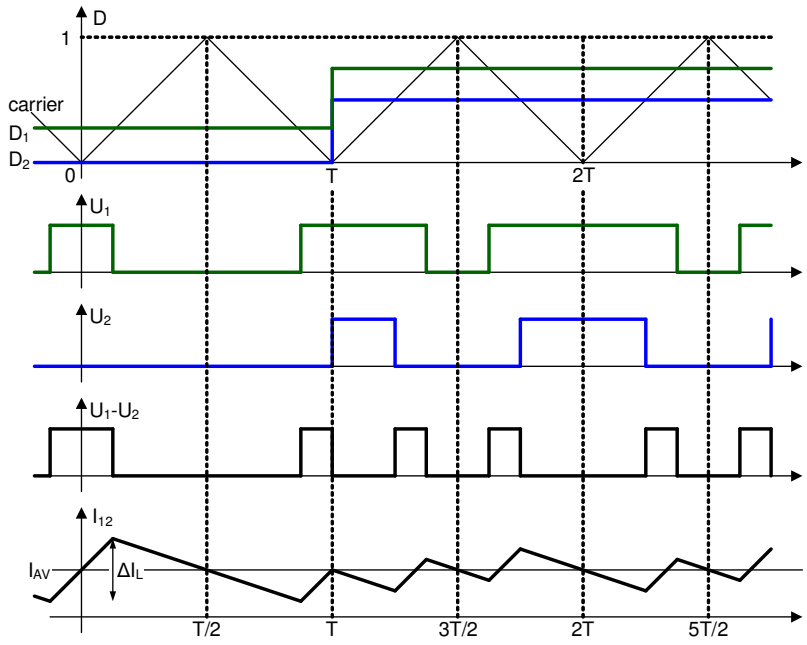


Figure 38. Waveforms for Type 2(a) zero sequence step

To get more understandable waveforms, it is advantageous to look at the phase-to-phase voltages and currents instead of the phase values. Figure 37 and Figure 38 show the carrier, duty ratios, phase voltages, phase-to-phase voltage and phase-to-phase current. Figure 37 shows these for two phases where one of the two is constantly switched to the DC rail before the zero sequence step, and the other is switched to the DC rail after the step. This case will be called the type 1 step. Figure 38 shows the case when both phases are switched after the zero sequence step; this will be called type 2 step. The voltages and currents are marked with the same labels as in Figure 35. It can be easily seen, that the mirror waveforms of these two waveforms are also possible. The type 1 waveform is symmetrical and its mirror image can be used if the phase of the carrier is inverted, but the type 2 waveform also has a (b) version because it will look different from Figure 38 if the carrier is at its maximum at the zero sequence step.

It can be easily understood, that in a flat-top modulated inverter for all zero sequence steps, one of the three phase-to-phase voltages will always perform a type 1 step, while the remaining two will perform type 2 steps. Looking at the waveforms of Figure 37 and Figure 38 it becomes clear that the rapid step in the zero sequence duty ratio in fact does change the phase-to-phase inverter voltage and inductor current waveforms. The change in the current waveform for the type 1 step is clearly such that the average current in the period of the zero sequence change will differ from the net average current value for a period. For the type 1

current waveform this is quite visible and is marked as I_{AV2} on Figure 37, but a similar effect can be observed also for the type 2 transition. The error causes a change in the average integral of the current as well. This integral has a dimension of charge. The physical meaning of this quantity is the voltage of the AC capacitor bank in the filter of a grid connected inverter, or the rotational speed of the motor in case of a drive. So that a voltage spike occours on the filter output for grid connected inverters, and torque pulsation appears in VFDs.

Not all discontinuous modulations suffer from harmonic problems. For example, the 120° Flat-Top modulation (also called dead-band) only leaves the bottom switch turned on in the unmodulated phase [61] and does not have steps in the zero sequence duty ratio, but causes uneven thermal dissipation among the semiconductors.

4.2. An empirical solution: the "BATMAN" modulator

Based on the waveforms of Figure 37 and Figure 38, the distortion can be clearly associated with the zero sequence step signal. If the zero sequence voltage changes slowly, then its spectrum is more flat and will result in less harmonics. With such signals, the current controller also has more time to intervene and correct distortion. I proposed a very simple empirical method based on this [C7], which was named as "BATMAN" modulator based ono the shape of the zero sequence waveform.

This method described below is based on the idea of reducing the slope of the step signal in the zero sequence duty ratio. This can be done by spreading the zero sequence transition in time, so that the whole transition takes longer than only one half switching cycle. This way, the high frequency content of the zero sequence voltage - and thus of the phase-to-phase voltage - can be significantly decreased. Leaving more time for the transition has additional advantages in current controlled systems, because the controller has time to intervene and correct some of the caused distortion.

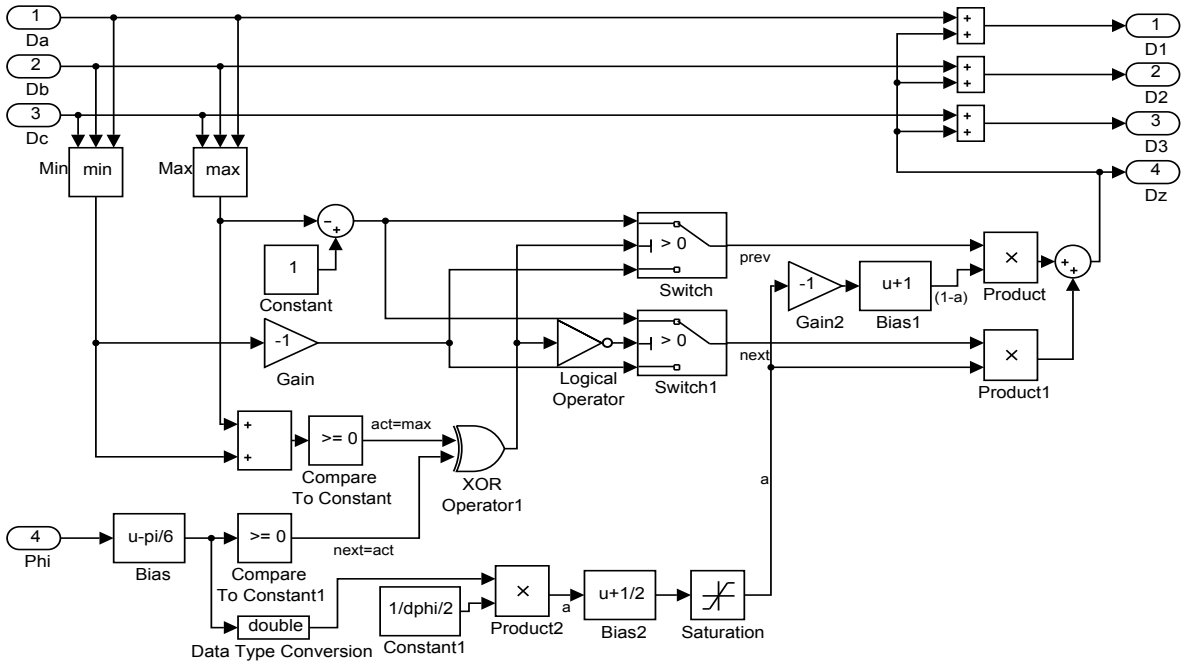


Figure 39. Block diagram of the "BATMAN" modified Flat-Top modulator

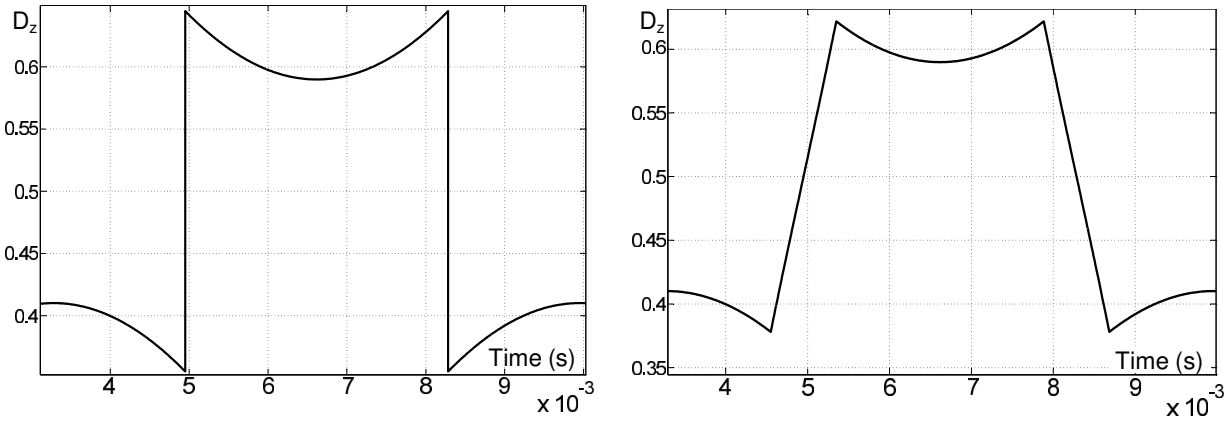
The intermediate duty ratio values were generated by the modified flat-top modulator seen in Figure 39. This realization of the modulator also uses a phase angle signal which shows the phase within the actual 60° block. So this value runs from 0 to π/6. A phase angle value is usually available in inverters so such a signal can be generated easily.

This modified flat-top modulator "BATMAN" contains an additional selection logic not present in the original flat-top. This selects not only the actual zero sequence duty ratio value, but during a zero sequence step, it also selects the duty ratio values before and after the transition. After the selection, a weighted average is calculated from the two selected values, using the properly offset, scaled, and saturated phase angle signal. The result is then used as the zero sequence duty ratio, and is added to the three inputs.

The *n* number of switching periods used for a transition can be set via the *dphi* parameter, which defines the phase angle region used for a transition. This can be calculated from the number of periods with the formula (3-1).

$$dphi = \frac{n \cdot f_1}{f_c \cdot 2 \cdot \pi} \tag{3-1}$$

In the formula above, the number of periods is marked with n, the triangular carrier frequency with f_c, and the fundamental output frequency with f_1. An example for the zero sequence duty ratio components (marked as Dz in Figure 39) for the original 60° flat-top modulation can be seen in 0. The average output voltage of the inverter has the same waveform with different scaling. An example for the Dz output of the new modulator can be seen on for n=2. It can be seen that apart from the transition, the waveform is the same as the original flat-top.



a. classical 60° flat-top

b. modified flat-top „BATMAN", n=2

Figure 40. Zero sequence duty ratio waveforms of original and modified flat-top modulators

The new "BATMAN" modulation scheme results in some decrease in efficiency. Normal Flat-Top modulation would have carrier frequency switching in only two of the three phase legs at all times (this is also classified as two-phase modulation in certain literature) and thus it has reduced switching losses. The "BATMAN" modulation uses PWM modulation in all three phases during each transition for a small n number of carrier periods (classified as three-phase modulation in certain literature), but two-phase modulation is used during the rest of the cycle. Three-phase PWM switching decreases converter efficiency, but it is used only for a short time. The theoretical efficiency can be calculated using the formula in (3-2) where η_2 is the efficiency with two-phase modulation, and η_3 is the efficiency with three phase modulation.

$$\eta = \left(\frac{f_c}{3 \cdot f_1} - n \right) \cdot \eta_2 + n \cdot \eta_3 \tag{3-2}$$

The decrease in efficiency is not very significant. It can be seen that a converter running at a carrier frequency of 6 kHz generating a 50 Hz sine wave uses 40 half periods for each 60°

output phase, of which only n = 2 or 4 need to be three-phase modulated with the modified modulation.

The modified flat-top modulator "BATMAN" was tested using the same simulation environment as described for Figure 36 in section 4.2 using 5 kHz carrier freqiency as well. The resulting waveforms using a higher n value can be seen in Figure 41. The resulting current spectrum for n=2 can be seen on Figure 42 for the first 40 harmonics. A significant reduction of the harmonics can be seen on Figure 42 compared to the spectrum seen in Figure 36(b), even though no current controller was used in the simulation environment. Only three fixed amplitude sine wave signals were sent to the modulator. The THD for the spectrum of 0 (n=2) is 0.0092. With increasing the n value to 4, this decreases further to 0.0046.

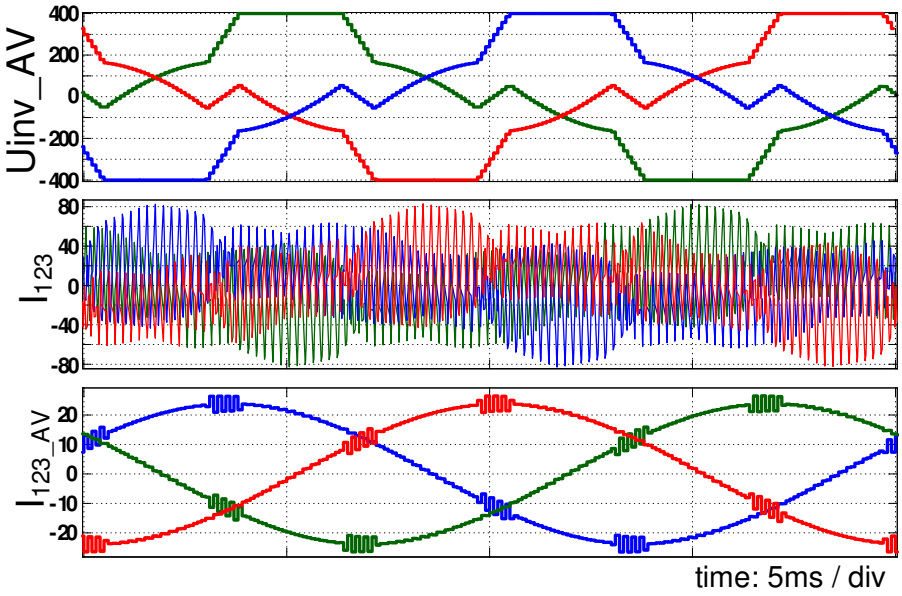


Figure 41. Average output voltages, actual and average currents for ideal inverters using the BATMAN modulator

It needs to be noted that even harmonics are present in the spectra because of assimmetry. This is well visible on the waveforms of Figure 36b. The sign and the magnitude of the error voltage and the current spikes is the same for any pair of φ and φ+π phase angles. The same is true for the waveforms on Figure 41. It was tested via simulation that the even harmonics disappear if the carrier frequency is changed to another value which is not a whole multiple of the fundamental output frequency.

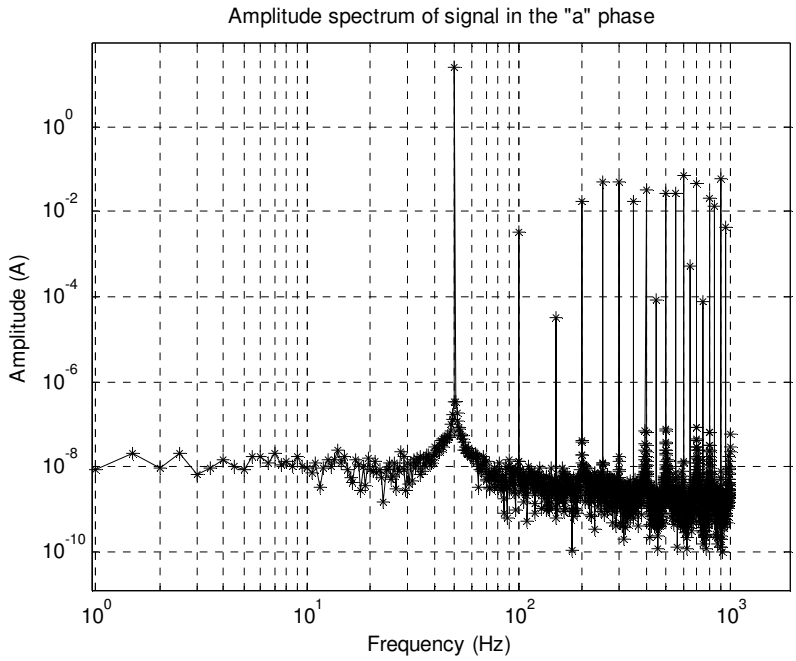


Figure 42. Current spectrum with the BATMAN modulator simulated with n=2.
This figure is directly comparable to Figure 36, the same power circuit parameters were used.

4.3. Analysis of the possible waveforms

The modified flat-top modulation scheme described in the previous section 4.2 for the compensation of distortion caused by Flat-Top transitions clearly has some drawbacks. Its main problem is that it does not produce two-phase modulated PWM signals at all times, and this results in increased losses when compared with the classical 60° Flat-Top modulation. A further goal of this research was to find a method which keeps all the efficiency benefits of the original 60° Flat-Top modulation by remaining a two-phase modulation. To achieve these goals, the actual transitions shown in Figure 37 and Figure 38 were further analyzed. During the analysis, the nomenclature of line voltages and currents already shown in Figure 35 with the delta capacitor bank were used. Furthermore, it was assumed that the frequency of the triangular carrier waveform is by orders of magnitude higher than the fundamental AC frequency ($f_{SW} >> f_1$), thus the change in grid voltage during a switching half-period was neglected.

Transition Type-1

The simplest Flat-Top transition (named as transition type-1) can be observed in phase pairs where one phase leg is connected to the DC bus before the transition, and the other one is connected to it afterwards. Figure 43 shows the original flat-top signals for two phase legs. The duty ratios of the three phase legs are marked as D_1, D_2, and D_3 in the figures respectively; these mark the ratio of the high side transistor ON time compared to the length of a full switching period; e.g. the duty ratio of the low side transistor in phase leg-1 is (1-D_1). In the figures D_{LL1} means the line duty ratio between the two phases undergoing a type-1 transition. At the actual phase angle shown in Fig. 3, $D_{LL1} = D_{13} = D_1 - D_3$. The u_{C13} voltage is positive and thus the i_{13} current increases if the triangular carrier waveform is between D_1 and D_3; otherwise the line current decreases. The peak-to-peak ripple of the line current can be calculated as follows:

$$\Delta i_{13} = \frac{\left(U_{DC} - U_{C_{13}}\right) \cdot D_{13} \cdot T}{2L} = \frac{U_{DC} \cdot \left(1 - D_{13}\right) \cdot D_{13} \cdot T}{2L} \tag{3-3}$$

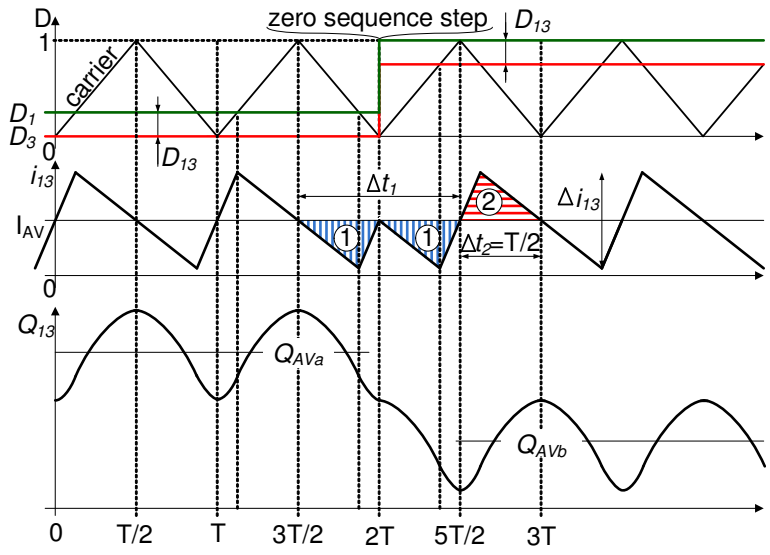


Figure 43. Original FLAT-TOP Waveforms at a phase angle for type 1 transition: PWM carrier, duty ratios, and the current and charge of one capacitor between two phases in delta configuration. $D_{LL1} = D_{13}$ at the actually shown phase angle.

In Figure 43 it can be seen that a 180° phase shift appears, so a positive half-period of the line current waveform is missing, resulting in an M- or W- shaped waveform depending on the

phase of the carrier. The integral of the i_{13} current during the Δt_1 time (the horizontally hatched red area ① in Figure 43) is two times larger during the time Δt_2 (vertically hatched blue area ② in Figure 43). The missing charge results in a change of the total charge on the capacitors of the filter, as shown in the example of Q_{13} in Figure 43. Applying the aforementioned assumptions, the resulting change in the capacitor voltage at the transition can be calculated as follows:

$$u_{C_{13}err} = \frac{Q_{①}}{C_{13}} = \frac{T \cdot \Delta i_{13}}{4C_{13}} = \frac{T^2 \cdot U_{DC} \cdot D_{13}\left(1 - D_{13}\right)}{8LC_{13}} \tag{3-4}$$

L in the equations (3-3) and (3-4) is the inductance of one phase of the low-pass filter, as shown in Figure 35. It can be noted that the voltage error shown in (3-4) is equal to the peak-to-peak switching frequency ripple voltage, and as such, the formula (3-4) is identical to (7-24) in [76]. As shown by (3-4), the error is more significant if L and C are small, and when the line AC voltage amplitude is close to 50% of U_{DC} (D_{LL1} = 0.5) at the transition (50% modulation index).

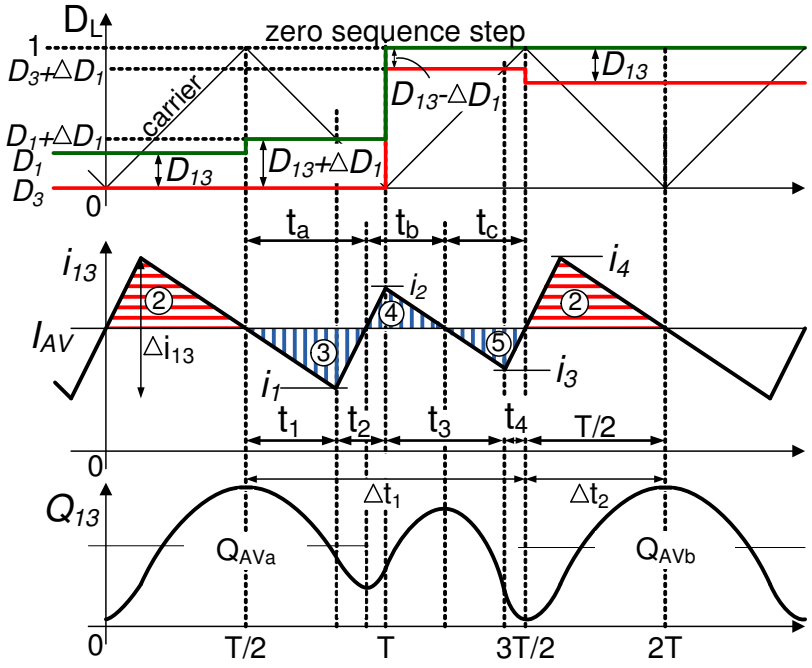


Figure 44. Compensated FLAT-TOP waveforms at a phase angle for type 1 transition: PWM carrier, duty ratios, and the current and charge of one capacitor between two phases in delta configuration. $D_{LL1} = D_{13}$ at the actually shown phase angle.

The goal of the compensation is to keep the average charge of the line capacitor the same for the preceding and succeeding half periods of the transition. The proposed method shown in

Figure 44 collapses the M- or W-shaped current waveform seen in Figure 43 by pushing it closer to I_{AV} (upwards in Figure 43). This is done by adding a compensation value ΔD_1 to the D_{LL1} duty ratio undergoing type-1 transition for the half period before the transition, and it is subtracted from it in the succeeding half period, leaving the average D_{13} unchanged. For this reason, as shown in Figure 44, the integral of the i_{13} current during the Δt_1 time (net area of ③-④+⑤, vertically hatched blue triangles in Figure 44) needs to be equal to the integral of the i_{13} current during the Δt_2 time (area ②, one horizontally hatched red triangle in Figure 44). This condition is expressed in the following equation (3-5):

$$\int_{\Delta t_1} i(t)\ dt = -\int_{\Delta t_2} i(t)\ dt = -Q_{②} = Q_{①} \tag{3-5}$$

This condition can be expressed for the waveform of Figure 44 in a system of equations. The set of equations used for determining the ΔD_1 compensation for type 1 transitions can be seen below, numbered separately from (3-T1-1) to (3-T1-13). The meanings of all variables are based on Figure 44. $i_1..i_4$ are referenced to I_{AV}. Equation (3-T1-13) represents condition (3-5).

$$U_{c13} = D_{13} \cdot U_{dc} \tag{3-T1-1}$$

$$t_1 = (1 - D_{13} - \Delta D_1) \cdot T/2 \tag{3-T1-2}$$

$$t_2 = (D_{13} + \Delta D_1) \cdot T/2 \tag{3-T1-3}$$

$$t_3 = (1 - D_{13} + \Delta D_1) \cdot T/2 \tag{3-T1-4}$$

$$t_4 = (D_{13} - \Delta D_1) \cdot T/2 \tag{3-T1-5}$$

$$i_1 = (-U_{c13} \cdot t_1) / (2L) \tag{3-T1-A6}$$

$$i_2 = i_1 + (U_{dc} - U_{c13}) \cdot t_2 / (2L) \tag{3-T1-A7}$$

$$i_3 = -(U_{dc} - U_{c13}) \cdot t_4 / (2L) \tag{3-T1-A8}$$

$$i_4 = D_{13} \cdot T/2 \cdot (U_{dc} - U_{c13}) / (2L) \tag{3-T1-A9}$$

$$t_a = t_1 + 2L \cdot (-i_1) / (U_{dc} - U_{c13}) \tag{3-T1-10}$$

$$t_b = T - t_a - t_c \tag{3-T1-11}$$

$$t_c = t_4 + 2L \cdot i_3 / (-U_{c13}) \tag{3-T1-12}$$

$$(T/2) \cdot i_4 / 2 = t_a \cdot (-i_1)/2 - t_b \cdot i_2/2 + t_c \cdot (-i_3)/2 \tag{3-T1-13}$$

This system of equations has been solved using the Symbolic Math Toolbox of MATLAB, to get the generalized solution for ΔD_1 shown in (3-6). In the generalized solution, the D_{13} line duty factor has been substituted for D_{LL1}. This can be done, as the formula itself is the same

for all six transitions of a period, provided that D_{LL1} is calculated correctly at each phase angle. The resulting formula can be seen below and is also plotted in Figure 45.

$$\Delta D_1 = \sqrt{\frac{D_{LL1} - D_{LL1}^{\ 2}}{2} + \frac{1}{4}} - \frac{1}{2} \tag{3-6}$$

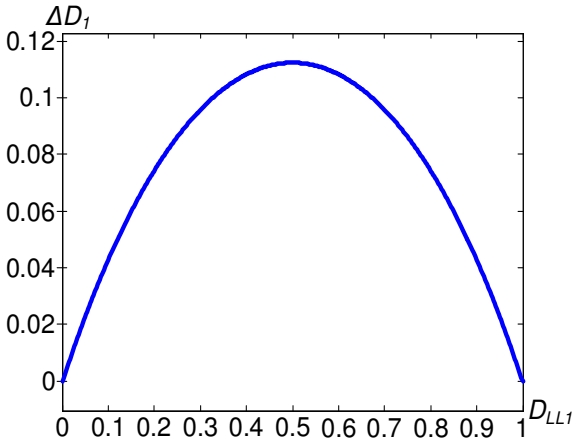


Figure 45. Calculated compensation for transition type-1.

As discussed at the beginning of the subsection, phase pairs in transition type-1 have one phase leg clamped to the DC bus before the transition, and the other is clamped to it afterwards. Figure 43 only shows the situation when clamping is to the negative DC bus before the transition, and it is to the positive bus afterwards. The mirror image of the waveforms in Figure 43 are also possible. In such cases ΔD_1 needs to be subtracted from the line duty ratio before the transition, and it needs to be added to it afterwards, but the formula for ΔD_1 remains the same. In fact, as one of the phase legs is always clamped in this waveform, ΔD_1 is only added to the duty ratio of one phase. This phase can be chosen by a compensation algorithm based on phase angle.

The other parameter not discussed before is the phase of the triangular carrier. The value of the carrier was zero at the transition on Figure 43, i.e. it was at its minimum peak. If the value of the carrier at the transition is one instead (at maximum peak), then compared to Figure 43, the i_{13} current becomes mirrored to the I_{AV} axis. In this case, in order to decrease the net area of the three triangles (①-②+③, vertically hatched blue area in Figure 43), the phase duty ratios need to be decreased by ΔD_1 instead of increasing. ΔD_1 is still calculated using the same formula (3-6).

Transition Type-2A

As each zero sequence transition takes place simultaneously in all three phases, the analytical solution described for type-1 transition also needs to be solved for the remaining two line voltages. In these waveforms, one phase is clamped to the DC bus on one side of the transition, and none of them is clamped to it on the other side. Such transitions were named as type-2. As the three line waveforms are not independent, it is sufficient to investigate only one of the remaining two. Based on the phase of the triangular carrier at a type-2 transition, two subtypes were identified: transitions with 0 carrier value at the transition were named as type-2A, and transitions at carrier value of 1 were named as type-2B.

The uncompensated type-2A transition waveforms can be seen in Figure 46. This figure shows the transition at the same phase angle as shown in Figure 43 (carrier is 0 at transition) but for phases 2 and 3. The line duty ratio participating in this transition is marked as D_{LL2}. At the phase angle shown in Figure 46, $D_{LL2} = D_{23} = D_2 - D_3$. As opposed to a type-1 transition, the type-2 transition waveforms are not symmetrical. Even though, a smaller asymmetrical M- or W-shape can still be recognized, as shown by areas ① and ⑥ in Figure 46.

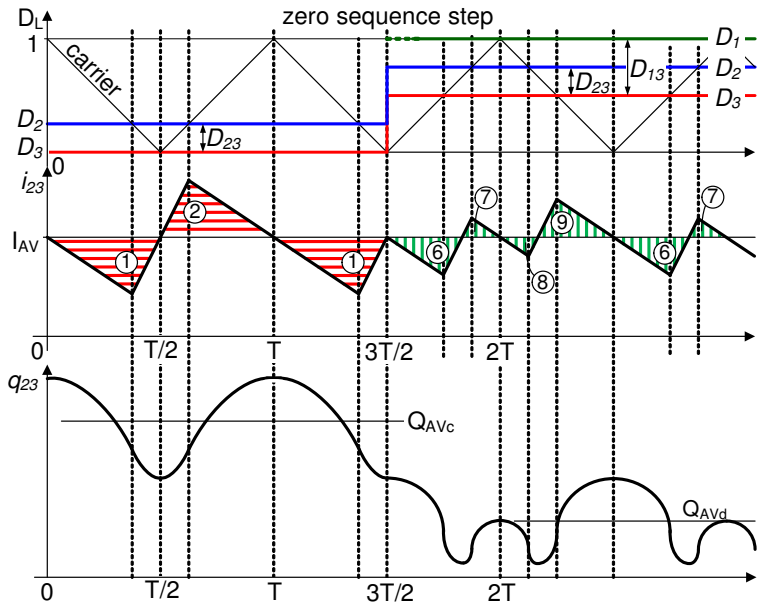


Figure 46. Transition type-2A waveforms at one phase angle: PWM carrier, duty ratios, and the current and charge of one capacitor between two phases in delta configuration. $D_{LL1} = D_{13}$, $D_{LL2} = D_{23}$ at the shown phase

The goal of the compensator in this case is to keep the average value of the charge q constant throughout the transition by collapsing the M- or W-shape towards I_{AV}. The operation of the compensation is shown in Figure 47. Here, the difference between the end- and the starting

points of the periodic *q(t)* waveforms on the two sides of the transition are marked as *ΔQ*. The *ΔQ* charge difference is the integral of the capacitor current for the two switching half-periods before and after the transition and can be calculated as the net area of the four diagonally hatched (blue) triangles shown in Figure 47. The value of this integral can be corrected by properly choosing the ΔD_{2A} compensation value. ΔD_{2A} is added to the actual line duty ratio D_{LL2} on one side of the transition and is subtracted from it on the other side.

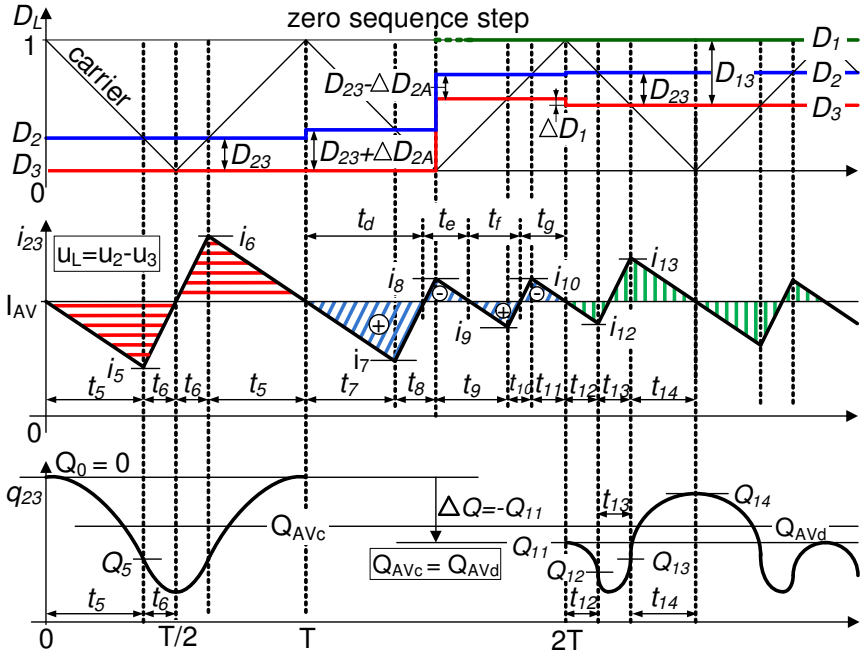


Figure 47. Transition type-2A compensated waveforms, directly comparable to Figure 46.

The waveforms of *q(t)* are built of parabolic segments. These had to be averaged on both sides of the transition for a half period, in order to be able to calculate the amount of *ΔQ* required for the compensation. This was performed using the formulae (3-7) to (3-9) shown below, where I_0 is the initial current and Q_0 is the initial charge at the beginning of the period:

$$i(t) = \frac{1}{\mathrm{L}} \int u \; dt = \frac{u \cdot t}{\mathrm{L}} + \mathrm{I}_0 \tag{3-7}$$

$$q(t) = \int i(t) \; dt = \frac{u}{2 \cdot \mathrm{L}} \cdot t^2 + \mathrm{I}_0 \cdot t + Q_0 \tag{3-8}$$

$$Q_{AV} = \frac{1}{\mathrm{T}} \cdot \int_{t}^{t+\mathrm{T}} q(\tau) \; d\tau = \frac{1}{\mathrm{T}} \left[\frac{u}{3 \cdot 2 \cdot \mathrm{L}} \cdot \tau^3 + \frac{\mathrm{I}_0}{2} \cdot \tau^2 + Q_0 \cdot \tau \right]_{t}^{\mathrm{T}} \tag{3-9}$$

The goal of the compensation, as shown in Figure 47, is defined as follows:

$$Q_{AVc} == Q_{AVd} \tag{3-10}$$

The complete set of equations required to get a formula for ΔD_{2A} can be found below numbered separately from (3-T2A-1) to (3-T2A-36). At first, a formula was obtained for the ΔQ charge difference by writing equations based on (3-9) and (3-10); these are equations (3-T2A-1) to (3-T2A-20) resulting (3-T2A-21). Then, the ΔD_{2A} intervention value had to be determined, which causes exactly the charge difference ΔQ. The equations (3-T2A-22) to (3-T2A-35) were obtained by calculating the net area of the four diagonally hatched (blue) triangles shown in Figure 47. The last equation (3-T2A-36) unifies (3-T2A-21) with the area calculations.

The actual equations are listed below. The meaning of the variables can be understood based on Figure 47. U_{c23} is the line voltage of the filtering capacitor. $Q_{AVc5\text{-}6}$ and $Q_{AVd7\text{-}9}$ are averages of parabolic segments. i_5 .. i_{13} are referenced to I_{AV}. At first, the durations t_5-t_6 and t_{12}-t_{14} of Figure 47 are defined as follows:

$$U_{c23} = D_{23} \cdot U_{dc} \qquad \text{(3-T2A-1)}$$

$$D_3 = 1 - D_{13} \qquad \text{(3-T2A-2)}$$

$$t_5 = (1 - D_{23}) \cdot \mathrm{T}/2 \qquad \text{(3-T2A-3)}$$

$$t_6 = D_{23} \cdot \mathrm{T}/2 \qquad \text{(3-T2A-4)}$$

$$t_{12} = \mathrm{T}/2 - t_{13} - t_{14} \qquad \text{(3-T2A-5)}$$

$$t_{13} = D_{23} \cdot \mathrm{T}/2 \qquad \text{(3-T2A-6)}$$

$$t_{14} = D_3 \cdot \mathrm{T}/2 \qquad \text{(3-T2A-7)}$$

Next, the average Q of the preceding waveform (one horizontally hatched red triangle of Figure 47) is determined:

$$i_5 = (-U_{c23}) \cdot t_5/(2\mathrm{L}) \qquad \text{(3-T2A-8)}$$

$$Q_5 = (-U_{c23})/2/(2\mathrm{L}) \cdot (t_5^2) \qquad \text{(3-T2A-9)}$$

$$Q_{AVc5} = 1/t_5 \cdot (-U_{c23}/6/(2\mathrm{L}) \cdot t_5^3) \qquad \text{(3-T2A-10)}$$

$$Q_{AVc6} = 1/t_6 \cdot ((\mathrm{U_{dc}} - U_{c23})/6/(2\mathrm{L}) \cdot t_6^3 + i_5/2 \cdot t_6^2 + Q_5 \cdot t_6) \qquad \text{(3-T2A-11)}$$

$$Q_{AVc} = 1/(\mathrm{T}/2) \cdot (Q_{AVc5} \cdot t_5 + Q_{AVc6} \cdot t_6) \qquad \text{(3-T2A-12)}$$

Then the same for the succeeding waveform:

$$i_{12} = (-U_{c23}) \cdot t_{12}/(2\mathrm{L}) \qquad \text{(3-T2A-13)}$$

$$Q_{12} = (-U_{c23})/2/(2\mathrm{L}) \cdot t_{12}^2 + Q_{11} \qquad \text{(3-T2A-14)}$$

$$i_{13} = (\mathrm{U_{dc}} - U_{c23}) \cdot t_{13}/(2\mathrm{L}) + i_{12} \qquad \text{(3-T2A-15)}$$

$$Q_{13} = (\mathrm{U_{dc}} - U_{c23})/2/(2\mathrm{L}) \cdot t_{13}^2 + i_{12} \cdot t_{13} + Q_{12} \qquad \text{(3-T2A-16)}$$

$$Q_{AVd12} = 1/t_{12} \cdot (-U_{c23}/6/(2L) \cdot t_{12}^3 + Q_{11} \cdot t_{12}) \quad (3\text{-T2A-17})$$

$$Q_{AVd13} = 1/t_{13} \cdot ((U_{dc} - U_{c23})/6/(2L) \cdot t_{13}^3 + i_{12}/2 \cdot t_{13}^2 + Q_{12} \cdot t_{13}) \quad (3\text{-T2A-18})$$

$$Q_{AVd14} = 1/t_{14} \cdot (-U_{c23}/6/(2L) \cdot t_{14}^3 + i_{13}/2 \cdot t_{14}^2 + Q_{13} \cdot t_{14}) \quad (3\text{-T2A-19})$$

$$Q_{AVd} = 1/(T/2) \cdot (Q_{AVd12} \cdot t_{12} + Q_{AVd13} \cdot t_{13} + Q_{AVd14} \cdot t_{14}) \quad (3\text{-T2A-20})$$

Solving (3-2TA-1) to (3-2TA-20) for Q_{11} results in the following formula:

$$Q_{11} = (D_{23} \cdot T^2 \cdot U_{dc} \cdot (D_{13} - 1) \cdot (D_{23} - D_{13} + 1))/(8 \cdot 2L) = -\Delta Q \quad (3\text{-T2A-21})$$

To realize the required $-\Delta Q$, ΔD_{2A} needs to be calculated. This has been done by calculating the areas of the four triangles around the transition in the current waveform (diagonally hatched blue areas in Figure 47.):

$$t_8 = (D_{23} + \Delta D_{2A}) \cdot T/2 \quad (3\text{-T2A-22})$$

$$t_7 = T/2 - t_8 \quad (3\text{-T2A-23})$$

$$t_9 = (D_3 + \Delta D_1) \cdot T/2 \quad (3\text{-T2A-24})$$

$$t_{10} = (D_3 + \Delta D_1 + D_{23} - \Delta D_{2A}) \cdot T/2 - t_9 \quad (3\text{-T2A-25})$$

$$t_{11} = T/2 - t_9 - t_{10} \quad (3\text{-T2A-26})$$

$$i_7 = -U_{c23} \cdot t_7/(2L) \quad (3\text{-T2A-27})$$

$$i_8 = i_7 + (U_{dc} - U_{c23}) \cdot t_8/(2L) \quad (3\text{-T2A-28})$$

$$i_{10} = U_{c23} \cdot t_{11}/(2L) \quad (3\text{-T2A-29})$$

$$i_9 = i_{10} - (U_{dc} - U_{c23}) \cdot t_{10}/(2L) \quad (3\text{-T2A-30})$$

$$t_d = t_7 + (2L) \cdot (-i_7)/(U_{dc} - U_{c23}) \quad (3\text{-T2A-31})$$

$$t_e = (2L) \cdot i_8 / (U_{dc} - U_{c23}) + (2L) \cdot (-i_8)/(-U_{c23}) \quad (3\text{-T2A-32})$$

$$t_f = (2L) \cdot i_9/(-U_{c23}) + (2L) \cdot (-i_9)/(U_{dc} - U_{c23}) \quad (3\text{-T2A-33})$$

$$t_g = (2L) \cdot i_{10}/(U_{dc} - U_{c23}) + t_{11} \quad (3\text{-T2A-34})$$

$$\Delta Q_{2A} = t_d \cdot i_7/2 + t_e \cdot i_8/2 + t_f \cdot i_9/2 + t_g \cdot i_{10}/2 \quad (3\text{-T2A-35})$$

$$-Q_{11} == \Delta Q_{2A} \quad (3\text{-T2A-36})$$

The line duty ratio D_{23} between the participating phases has been substituted for D_{LL2} and D_{13} has also been substituted for D_{LL1} in the generalized formula (3-11), as the formulas are independent of the actual phase angle if D_{LL2} and D_{LL1} are calculated properly. In the compensation algorithm, a sector table can take care of this, which will be shown in section 4.4. The sets of equations were solved using the Symbolic Math Toolbox of MATLAB. The closed formula for ΔD_{2A} can be seen below:

$$\Delta D_{2A} = \frac{-D_{LL2} \cdot (D_{LL2} - k + D_{LL1}^{\ 2} - D_{LL2} \cdot D_{LL1})}{4D_{LL2} - 2D_{LL1} + k + 1} \tag{3-11}$$

Part of the formula has been extracted as k to decrease the required computation time:

$$k = \sqrt{-2D_{LL1}^{\ 2} + 2D_{LL1} + 1} \tag{3-12}$$

The formula (3-11) for ΔD_{2A} has been plotted in Figure 48. As shown in Figure 46, D_{LL2} is always smaller than D_{LL1}, so the contour diagram of ΔD_{2A} shown in Figure 48 has only been evaluated for $D_{LL1} > D_{LL2}$.

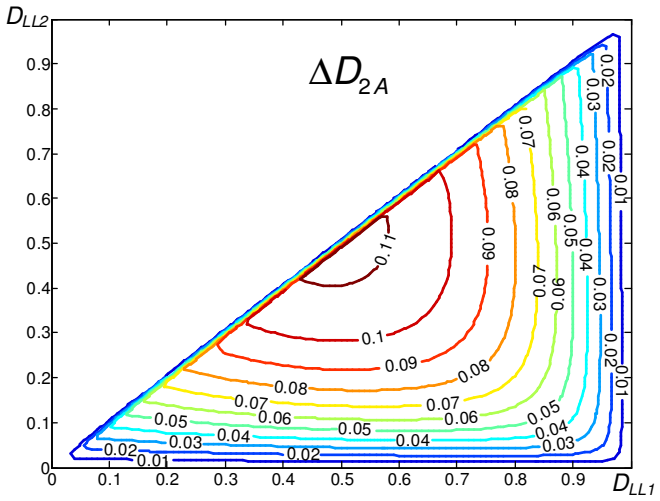


Figure 48. Contour diagram of compensation (ΔD_{2A}) for type-2A transitions.

It needs to be noted that although only one direction of the 2A transition has been investigated (one phase clamped before and no phase clamped after the transition), the calculated ΔD_{2A} function shown in (3-11) can also be used in the other direction. In such cases, all waveforms in Figure 46 are flipped around the vertical axis, so ΔD_{2A} needs to be subtracted from the line duty ratio for the half period before the transition, and it needs to be added to it afterwards.

Transition Type-2B

As discussed in the previous section, clamped to unclamped or unclamped to clamped transition may also happen when the carrier is at 1 instead of 0. These were named as type-2B transitions. Although the inversion of the carrier phase at the transition is the only difference from type-2A transitions, the waveforms are different from the ones shown in Figure 46, so the formula (3-11) cannot be used. A different compensation value ΔD_{2B} is required instead.

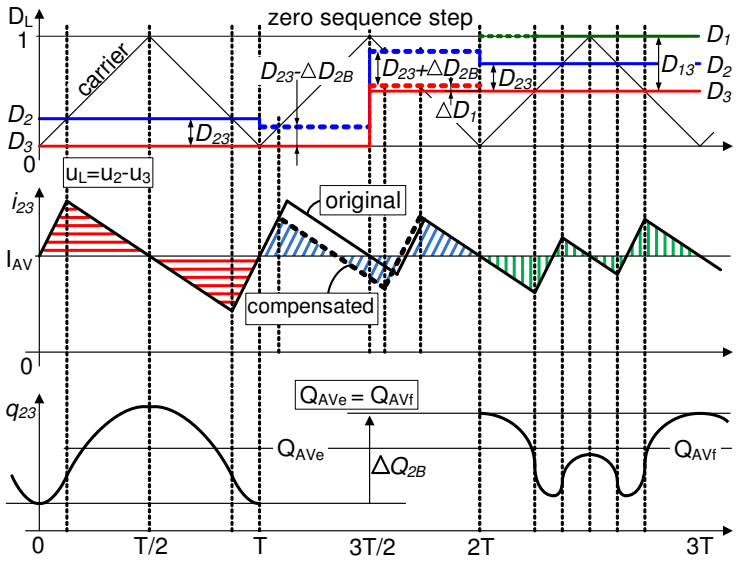


Figure 49. Transition type-2B original (continuous) and compensated (dashed) waveforms.

The original and the compensated type-2B transition waveforms can be seen in Figure 49. The method of writing the systems of equations and calculating the compensation formulae for type-2B transitions is the same as described for the type-2A: the compensator keeps Q_{AV} constant on the two sides of the transition. The detailed formulas are not included here, they would provide no additional information as the way of creating them was the same as for the (3-2TA-1) to (3-2TA-20). The solution for the system of equations is in (3-13) as follows:

$$\Delta D_{2B} = \frac{-D_{LL2} \cdot (2D_{LL1} - D_{LL2} + k - D_{LL1}^{\ 2} + D_{LL1} \cdot D_{LL2} - 2)}{2D_{LL1} - 4D_{LL2} + k + 1} \tag{3-13}$$

The resulting formula is similar to (3-11) and the same k can be extracted from it as in (3-12). The results of formula (3-13) have been plotted on a contour diagram in Figure 50.

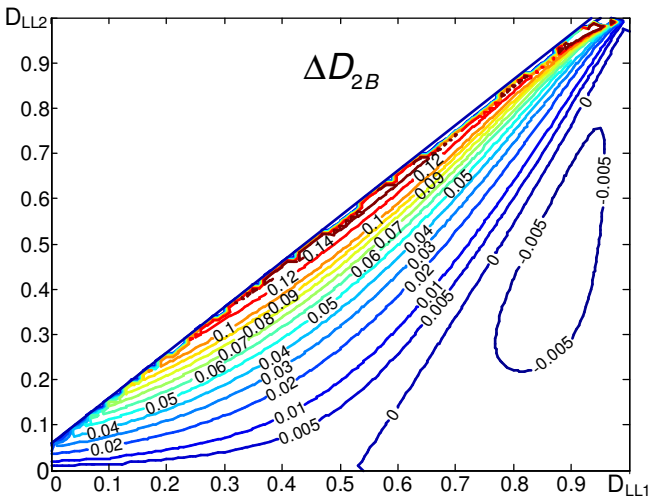


Figure 50. Contour diagram of compensation (ΔD_{2B}) for type-2B transitions.

4.4. Analytical compensation algorithm, Results

In the previous section 4.3, it has been shown that the three formulas (3-6) (3-11) and (3-13) can be used for keeping the average AC capacitor charge constant through 60° flat-top transitions. The actual algorithm using these formulae can be designed based on Figure 43, Figure 46 and Figure 49.

In practice, the control algorithms of PWM inverters are usually implemented in interrupt routines which run once in every half period, as shown in Figure 51. In one such interrupt routine, the A/D conversion results of current and voltage values sampled at the previous peak of the triangular carrier are already available. Here the DSP needs to run the control and modulation algorithms and set the phase leg duty ratio values for the next half period.

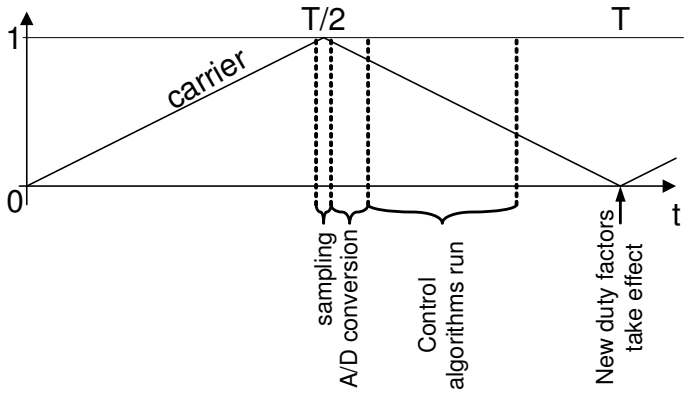


Figure 51. Timing of the control software.

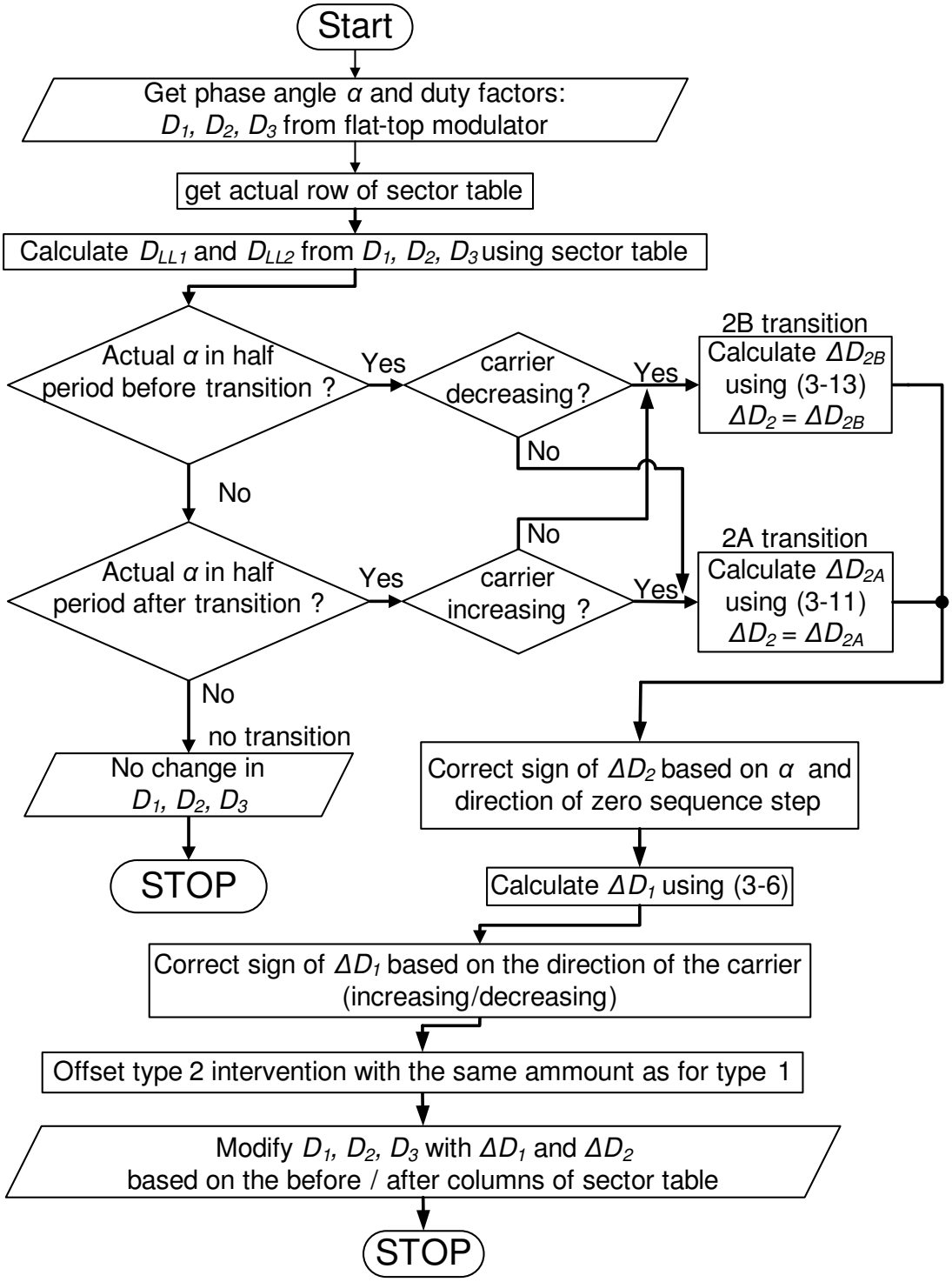


Figure 52. Flowchart of the compensation routine run once in every half-period.

The flowchart of the actual flat-top compensation algorithm can be seen in Figure 52. This takes its input from the original flat-top modulator in the form of three phase leg duty ratios. The compensator modifies these duty ratios only if the next duty ratios taking effect will be valid for a half period immediately before or after a 60° flat-top transition. This is determined from the actual phase angle α and the discrete angular frequency α_step that describes how

much α changes in a half-period. The previous, the actual, and the next sector can be selected based on the phase angle α. α and α_step are also used to decide if the actual half period being processed is immediately before or after a 60° transition, or just at the middle of a sector requiring no intervention. The compensator selects one row of the sector table shown in TABLE IV based on the actual sector. This contains information about how to calculate the line duty ratios D_{LL1} and D_{LL2} from the phase leg duty ratios, and shows which phases undergo type-1 and type-2 transitions.

TABLE IV SECTOR TABLE FOR TRANSITION DEPENDENT PARAMETERS

Phase	Type 1.			Type 2.		
α [a]	D_{LL1} from phase [b]	Add ΔD_1 to D_x before transition [c]	Add ΔD_1 to D_x after transition [c]	D_{LL2} form phase [b]	Zero sequence step direction	Add ΔD_2 to D_x [c]
0°	1-2	1	2	3-2	+	3
60°	1-3	3	1	2-3	-	2
120°	2-3	2	3	1-3	+	1
180°	2-1	1	2	3-1	-	3
240°	3-1	3	1	2-1	+	2
300°	3-2	2	3	1-2	-	1

[a] α is such that $D_{L1} = 1/2 + \cos(\alpha)/2$

[b] e.g. $D_{LL1} = D_1 - D_2$ and $D_{LL2} = D_3 - D_2$ for a transition at α=0°

[c] the value of the phase index „x” is listed in the column below

If compensation is required in the actual half-period, the compensator calculates ΔD_1 for type-1 compensation. The sign of the result needs to be corrected if the transition happens at a carrier level of 1, because (3-6) has been calculated based on Figure 43 where the transition is shown with carrier at 0 (minimum peak). Next, the compensator decides whether a type-2A or a -2B compensation should be performed, based on the phase of the carrier at the transition (0 for minimum or 1 for maximum peak) and whether the following half period will precede or succeed the transition. The latter can be decided from phase angle α. As shown in Figure 46 and Figure 49, ΔD_2 correction is added to the same phase leg duty ratio for type 2 transitions

both before and after the transition, but the direction of the correction (sign) is different. As the compensation has been calculated for positive zero sequence steps in (3-11) and (3-13), the sign of ΔD_1 also needs to be inverted for negative zero sequence steps shown in TABLE IV.

After all modifications have been performed to ΔD_1 and ΔD_{2A} or ΔD_{2B} (shown as ΔD_2 in Figure 52), the correction offsets are added to the phase leg duty ratios shown by the sector table. The type-1 correction ΔD_1 is added to a different duty ratio before and after the transition, while the type-2 correction ΔD_2 is added to the same one in both half periods.

Simulation results

The full compensation method shown in Figure 52 has been tested first in Matlab Simulink environment. The simulated inverter was run stand-alone in open-loop control with an LC filter of 1mH per phase and 3uF capacitance between phases, in delta configuration. The simulation was run from 60V DC at no load, generating 30V amplitude line voltage. The fundamental frequency was set to 45.6621Hz because of practical reasons to have synchronous modulation at 10kHz PWM carrier frequency and minimum rounding error in the phase angle when stepped twice per switching period. Steady state synchronous modulation was only useful to make the waveforms easier to reproduce and measure on real hardware using an oscilloscope, as described later in the next section. The values described above were purposefully chosen to be the same as for the low power inverter described in the next section to produce comparable results.

The compensation algorithm described in the paper has been realized in a triggered Simulink block. The simulated inverter was assumed ideal, with no delays, control dead time, or voltage drop. The resulting transition waveforms of the line currents and voltages using the original flat-top modulation without compensation can be seen in Figure 53. The waveforms are easily comparable to those in Figure 43: the W-shape is easily recognizable, and the change in the filtering capacitor line voltage is also similar to the drawing based on the theoretical explanation. The main difference is that the change in the output capacitor voltage, caused by the lost charge during the transition, initiates an oscillation. The proper operation of the compensation algorithm can be seen at the same transition in Figure 54. It is visible, that apart from the fundamental component, the results are identical to the theoretical waveforms

of Figure 44. It is also visible that the correction of the disturbance caused by the lost charge throughout the transition also eliminates the oscillation seen in Figure 53.

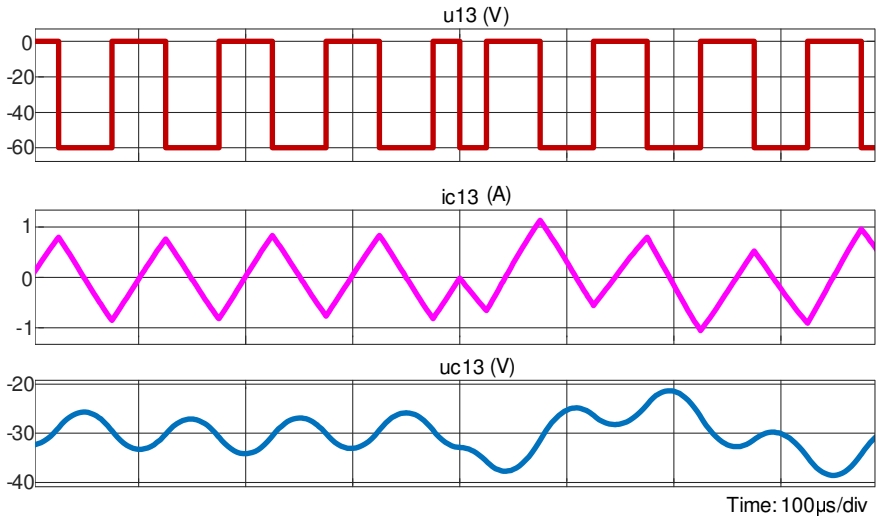


Figure 53. Simulated type-1 waveforms without compensation.

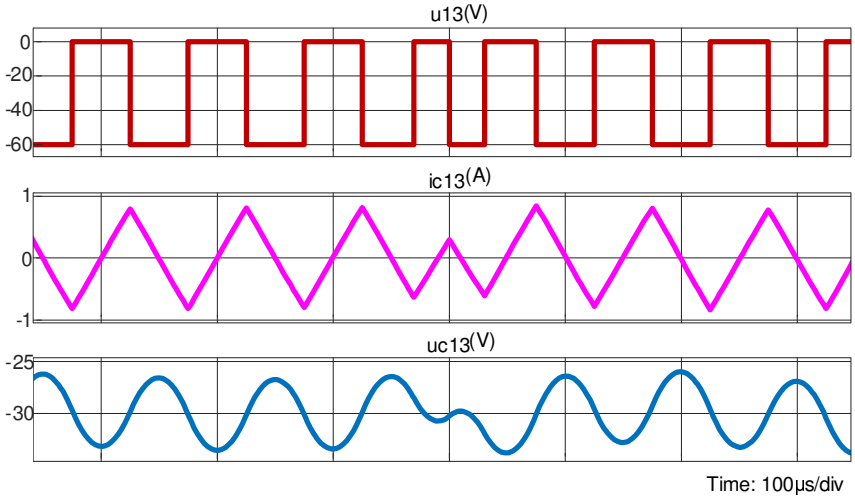


Figure 54. Simulated type-1 waveforms with compensation.

Experimental results with a low power inverter

The new compensation algorithm has been tested on two different systems. A low power MOSFET-based inverter was used first; this is favorable for experimenting because of its low cost and ease of performing modifications. This enabled a large number of software and filter configurations to be easily tested.

The methodology described has been first experimentally tested on an extra low voltage modular power electronics test bench called AMER shown in Figure 55. The system has been

developed at the Department of Automation and Applied Informatics of the Budapest University of Technology and Economics for educational and research purposes. It can be supplied by a 80V DC bus with up to four two-level MOSFET-based phase leg modules, each having isolated gate drivers, hall-effect current measurement, and a separate protection CPLD. The controlling CPU card contains a Texas Instruments TMS320F28069 DSP and a CPLD for additional flexibility.

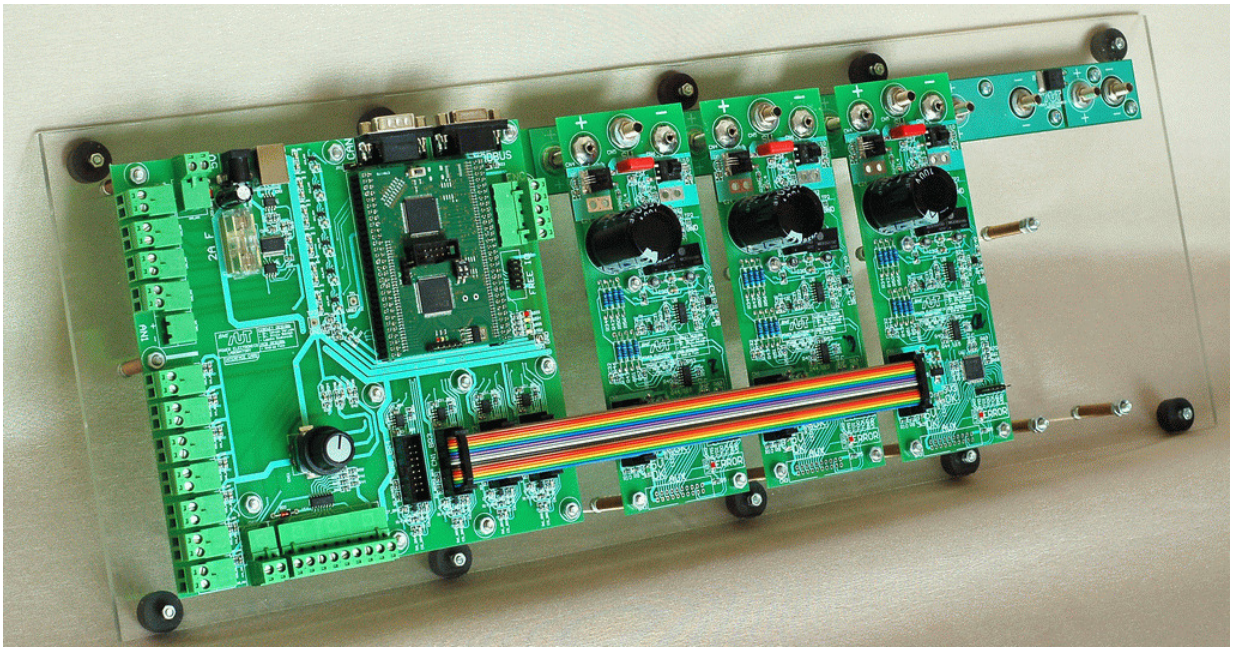


Figure 55. AMER extra low voltage power electronics test bench,
shown with three phase leg cards.

The new Flat-Top compensation algorithm has been programmed for the DSP in C language using TI Code Composer Studio. A PWM carrier frequency of 10 kHz was used during the tests. Inductors in all filter configurations were 1mH single phase ferrite chokes. The output filtering capacitor bank was built of three 1µF foil capacitors connected in delta. These inductor and capacitor values are somewhat low for the 10kHz switching frequency: an LC filter with these has resonance at 2.9kHz, and an LCL filter has an additional resonance at 4.1kHz. Low value filter components are often used because of cost reasons, and function well in certain applications. The problem is that without sufficient damping, transients from uncompensated Flat-Top transitions may cause oscillations and increased harmonic emissions. The effect of compensation is therefore most visible with underdamped filters and low ohmic loads.

In the first test the inverter was run stand-alone in open-loop control with LC filter from 60V DC at no load, generating 30V amplitude line voltage. The fundamental frequency was set to 45.6621Hz to have synchronous modulation at 10kHz switching frequency. This was not required for the compensator, but it made easier to set the oscilloscope and take the resulting waveforms seen in Figure 56 and Figure 57. The u_{13} capacitor voltage was measured by a Hameg HZ100 differential voltage probe, and the current was measured using a Tektronix P6302 current probe via AM503A amplifier. The data was recorded on a Rhode & Schwarz RTO1004 oscilloscope. The DC bus was supplied from a Matrix MPS-3005L-3 power supply. The resulting waveforms in Figure 57 are easily comparable to Figure 43 and Figure 44, because those figures were drawn based on the assumption that the load currents are constant through one switching period. This is fulfilled if there is no load, as the output currents of the filter are zero.

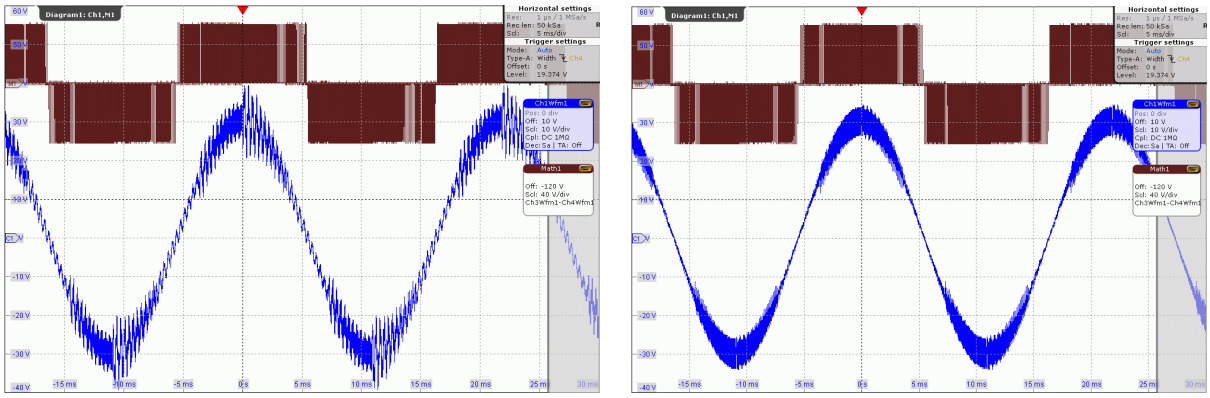


Figure 56. Voltage waveforms measured on unloaded stand-alone inverter.
Original (left) and compensated (right). Top (Math1): u_{13} (voltage between phase legs).
Bottom (Ch1): u_{c13} (voltage of delta capacitor).

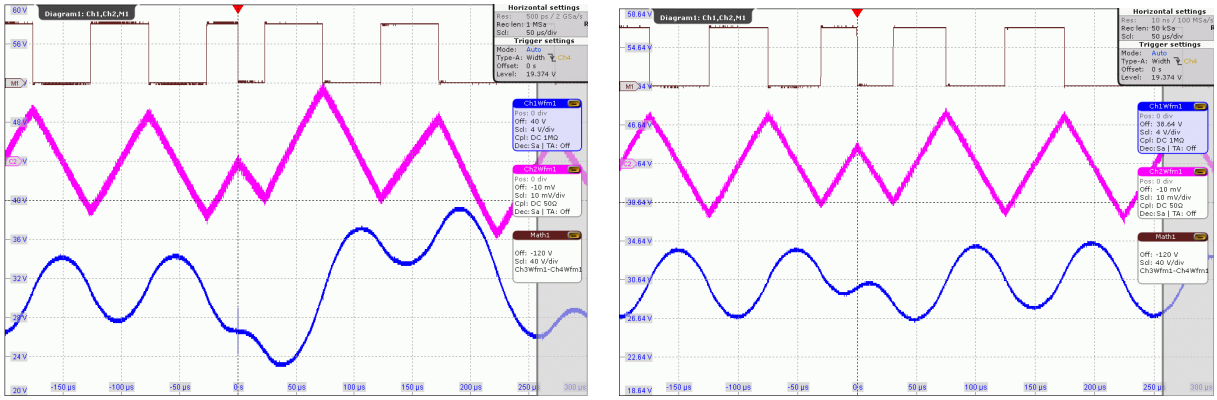


Figure 57. Same as in Figure 56, with the transition at the trigger point magnified. Original Flat-Top (left) and compensated (right) Top (Math1): u_{13} (as in Figure 56). Middle (Ch2): i_{c13} current of one delta capacitor. Bottom (Ch1): u_{c13} (as in Figure 56)

As the measurements were performed without resistive load, the oscillations caused by the transitions dampen slowly in Figure 56. The odd harmonics spectrum of the capacitor voltage u_{13} for the unloaded stand-alone inverter calculated via FFT for one period can be seen in Figure 58. The asterisks (blue) show the results for the uncompensated voltage, and the dots (red) show results with the new compensation method. The increase of distortion around the 219th harmonic is due to the 10kHz switching frequency. The effectiveness of the compensator lies in the higher harmonic orders, most visible above the 40th harmonic, in the so called supraharmonic range. Most current standards and guidelines of harmonic emissions only cover frequencies up to the 40th or 50th harmonic [78], while some planned standards use a 9 kHz limit of low frequency harmonic emissions, and include frequencies up to 150 kHz [79][80]. Calculating the THD for the first 40 harmonics shows a reduction from 1.21% to 0.63%. Calculating the THD up to the 9 kHz limit (197th harmonic in this case) reduces from 11.17% to 1.94%.

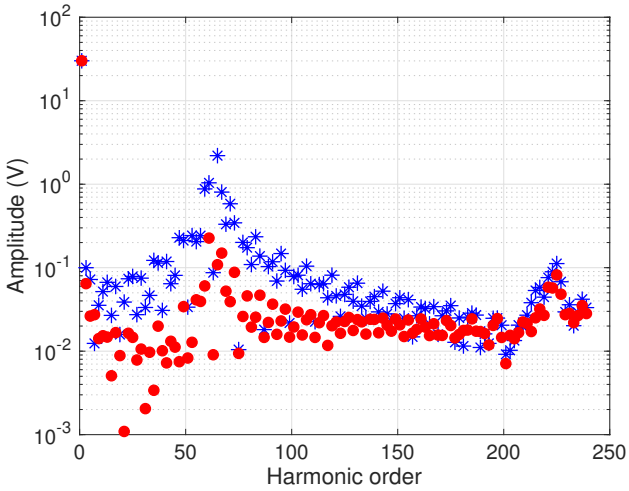


Figure 58. Odd harmonic spectrum of the U_{13} capacitor voltage. Stand-alone inverter without compensation (blue asterisk) and with compensation (red dot) at no load

As described before, additional experiments were also conducted to demonstrate the operation of the method in the more realistic grid-connected configuration, using DQ current control. This measurement setup is shown in Figure 59 and a photo can also be seen in Figure 60. The low voltage inverter was run from a 65V DC bus, and was connected to the 230V three phase AC grid through three 24V/230V toroidal transformers (inside the three boxes in the background of Figure 60) and a three phase variac autotransformer set to 50% (on the bottom right in Figure 60) to simulate a 12V three phase grid. Synchronization was performed via software PLL.

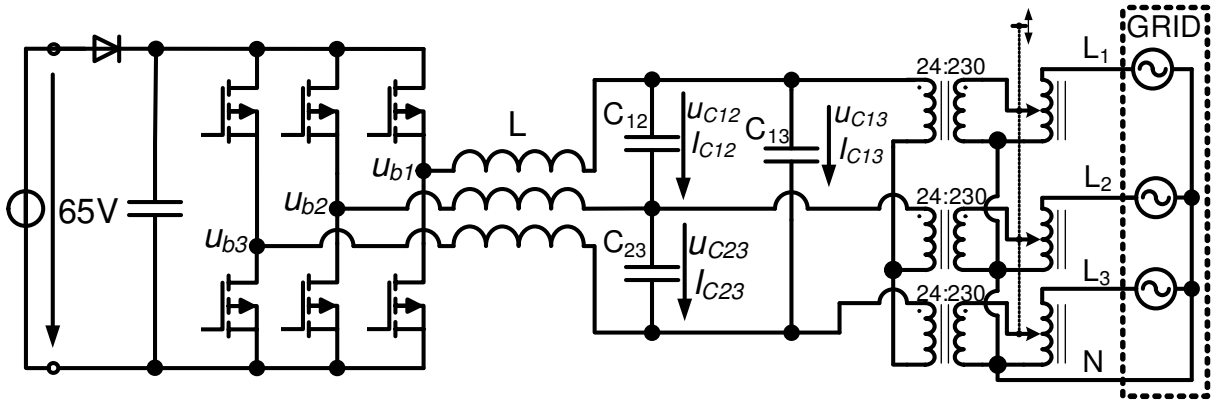


Figure 59. Power circuit of the laboratory setup of the grid-connected low voltage inverter. Analog voltage and current sensors and MOSFET gate control signals are not shown.

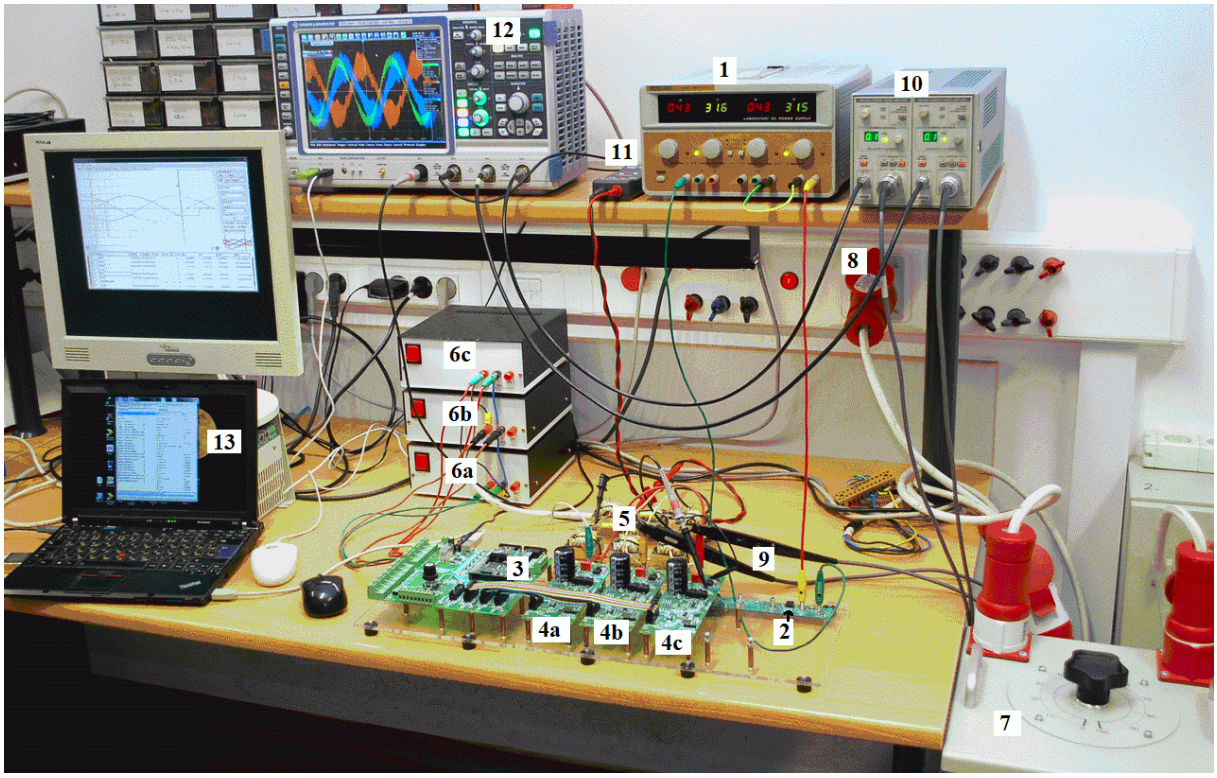
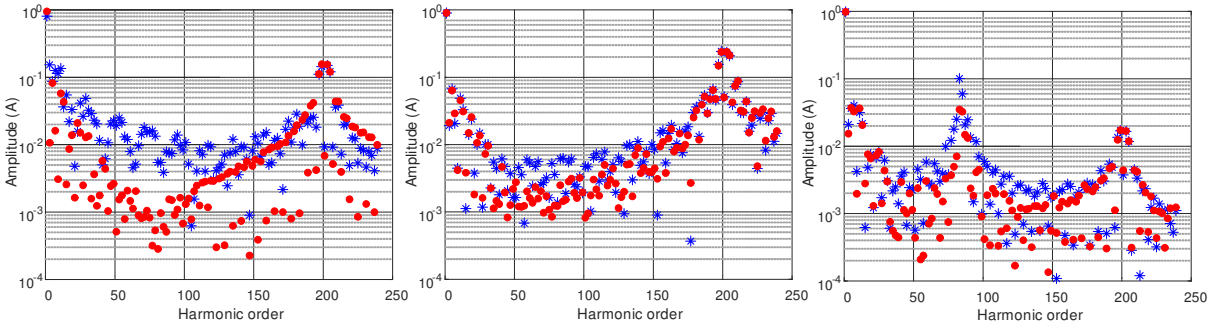


Figure 60. Photo of the laboratory setup of the grid-connected low voltage inverter.

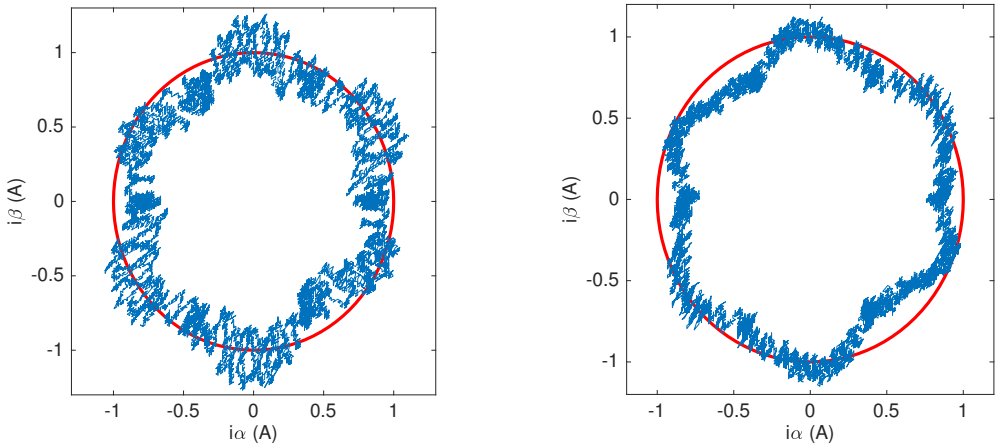
1: Matrix MPS-3005L-3 DC power supply, all outputs in series.
2: diode on DC bus. 3: inverter control card with TMS320F28069 cpu.
4a, 4b, 4c: phase leg cards of three phase inverter (one per phase)
5: LC filter arrangement. 6a, 6b, 6c: toroidal transformers with 24:230 ratio
7: three phase variable autotransformer (variac).
8: three phase grid connection. 9: Tektronix P6302 current probes
10: Tektronix AM503A amplifiers. 11: Hameg HZ100 differential voltage probe
12: Rhode & Schwarz RTO1004 oscilloscope
13: laptop computer with external monitor, running monitoring software with watch window and recorder (oscilloscope) functionality.

The current reference for the active current component was set to 1A peak fundamental phase current, and for the reactive component it was set to zero. Even though the analysis of the waveforms were performed assuming the presence of an ideal LC filter, the linear nature of such an LC filter means that harmonics present at the output of the filter must have been already present before the filter, directly at the output of the inverter phase legs. This means that a method reducing the amplitude of harmonics after the LC filter should also have reduced the amplitude of these harmonics at the output of the inverter and this should have an effect even if other filter configurations are used as long as those filters are also linear. Based on this idea, tests were performed with L, LC, and LCL filters as well. The resulting spectra of currents measured on the outputs of the filters can be seen in Figure 61. The blue asterisks show the measured harmonics present without compensation, and the red dots show the harmonics with compensation. The three phase grid voltage of the building has already contained several harmonics at the time of the measurement, and these are also well visible in the current. As a result, the actual values are not very relevant, but the reduction in the harmonic contents is visible. The current THD values calculated up to 9 kHz show a reduction from 58.2% to 12.9% for the L filter, a 14.0% to 12.8% for the LC filter, and 15.8% to 9.1% for the LCL filter. This together with the spectra in Figure 61 show that higher order filters remove more of the wideband noise generated by the flat-top transitions, but may have oscillatory response at certain frequencies.



A: L filter B: LC filter C: LCL filter

Figure 61. Grid current odd harmonic spectra with various filters without (blue asterisk) and with compensation (red dot)



A. Compensation disabled B. Compensation enabled

Figure 62. Space vector diagram of the grid current of LCL filtered inverter without (A) and with (B) compensation. The ideal circle (red) is shown for comparison.

In [77] R.K. Jardan et al. published a paper about the space vector application in the field of analysis of three phase power electronics converters. Using the described methods, the grid current of the LCL filtered inverter has also been evaluated on space vector diagrams. These were recorded via measuring two phase currents using two current probes and amplifiers, as seen in Figure 60. The results were transformed to space vectors and were plotted using MATLAB in Figure 62. The reduction of harmonic currents is well visible when comparing the blurriness of the hexagons. The deviation of the space vector time function trajectory from the ideal circle can be caused by the low order harmonics and negative sequence components present in the grid voltage (probably from a large three phase diode rectifier in the building), which are also present in the current because of the slow controllers.

Experimental results with a high power inverter

Testing on a miniature MOSFET inverter had many practical advantages, but large IGBT based inverters usually have slower switching speeds and different dynamic behavior. As such, an additional measurement has been performed with modified software on a 50kW inverter used in the active rectifier stage of an electric car fast charger seen in Figure 63. The compensation algorithm was compiled into the existing control software of the system which runs on a Texas Instruments TMS320F28335 DSP.

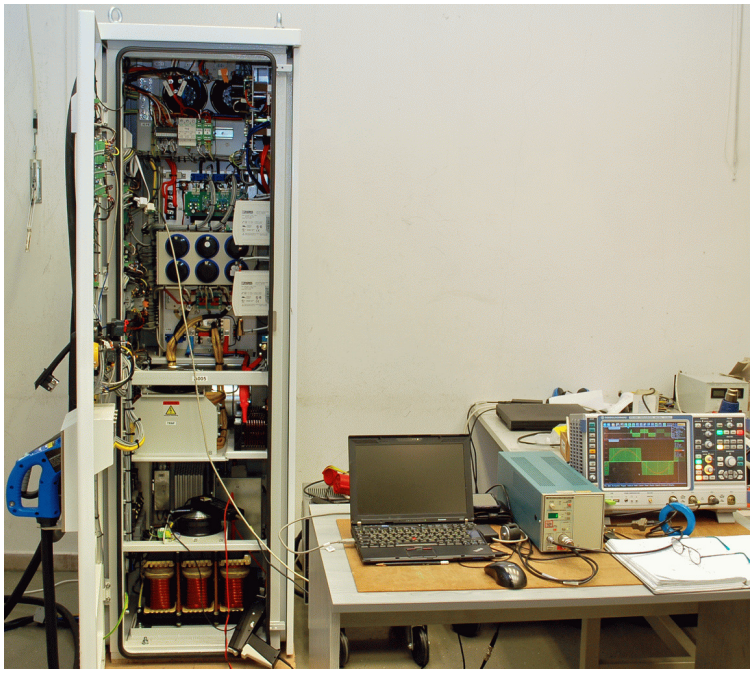


Figure 63. Laboratory tests on the Procon eDC-S01 50kW CCS / CHAdeMO compatible electric car fast charger

In the test, the inverter of the active rectifier stage was disconnected from the grid at no load and was run at 10kHz switching frequency generating 50Hz three phase symmetrical voltage. The DC bus was 600V supplied by the built-in precharging unit which has its own isolation transformer and diode rectifier. The LC low pass filter of the inverter consisted of a 400µH inductor and 20µF capacitor in star connection for each phase. The filter has also included two series RLC notch filters parallel to each grid side capacitor. These were tuned for 10kHz and 20kHz frequencies to conform EMC standards. The software was configured to ramp up the peak AC line voltage to 300V. The voltage between two phase legs has been measured using a Tektronix P5200 differential probe, and the output line voltage of the inverter was measured using a Hameg HZ100 differential probe. The data was recorded on a Rhode & Schwarz RTO1004 oscilloscope.

The measured voltage waveforms without and with compensation can be seen in Figure 64 as recorded by the oscilloscope. The data was saved in CSV format and was further processed in Matlab. The spectrum up to the first 240 harmonics can be seen in Figure 65. A resonance of the LC filter is visible near 1800 Hz (36th harmonic). The THD of the output line voltage calculated for the first 40 harmonics has been decreased from 3.84% to 0.48% by the compensator. For the first 9 kHz, a THD reduction from 3.96% to 0.53% was measured.

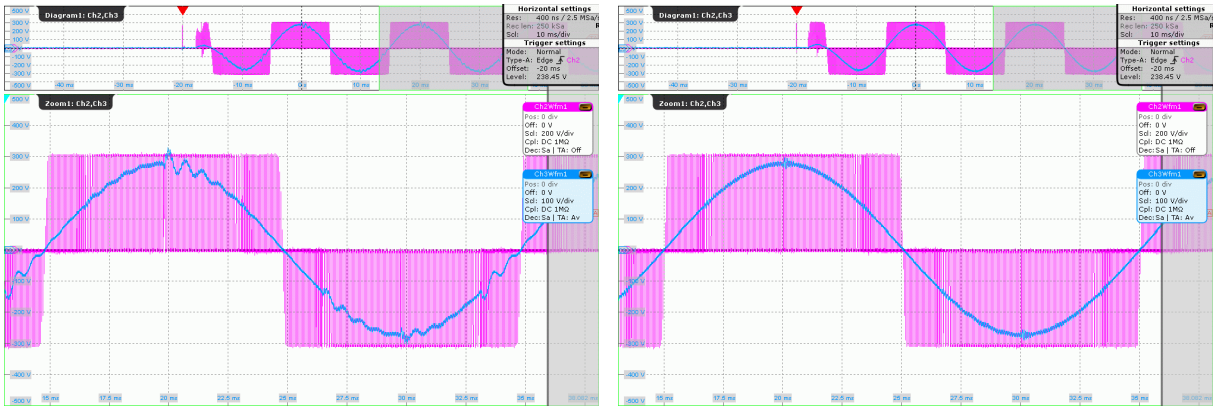


Figure 64. Voltage waveforms measured on unloaded stand-alone inverter shown in Figure 63. Original (left) and compensated (right). Ch2 (pink): u_{13} (voltage between phase legs). Ch3 (blue): u_{c13} (line voltage on capacitor bank).

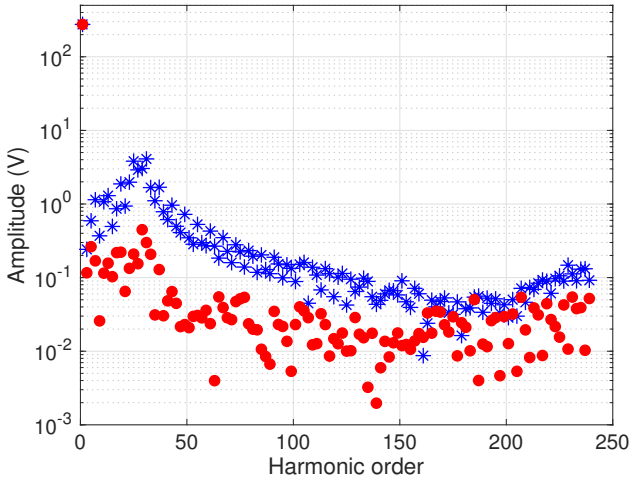


Figure 65. Odd harmonic spectrum of the waveforms of u_{c13} from Figure 35 without compensation (asterisk) and with compensation (dot)

4.5. New scientific result – Thesis 3:

Based on theoretical analysis and measurements, the following can be stated as thesis 3:

I have shown that the output current of 60° FLAT-TOP modulated inverters has an incorrect value for one switching period at every zero sequence step. I have identified the current and voltage waveforms caused by the step in LC filtered three phase inverters. I have shown how to calculate the duty ratios required for minimal distortion in each phase. Based on the resulting formulae, I have defined a method to decrease harmonic emissions caused by FLAT-TOP modulation. I have shown that the efficiency of a converter using the new compensated modulation is not worse than with using the original FLAT-TOP modulation.

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5. Conclusion

Our modern electrical grid connects to increasing numbers of PWM modulated voltage source inverters used as both generating units and loads. Close to linear operation of such inverters is important from an EMC standpoint. This means keeping the amplitude of harmonic current emissions and radio frequency current- and voltage components low. As modern inverters often use increased switching frequencies, the size and value of the associated passive filter components is often reduced so that they do not filter low order harmonics efficiently any more. As such, the amplitudes of harmonic current components can only be reduced by software methods. This mostly means identifying the actual causes behind harmonic emissions and compensating for them. The research work related to the theses and described in the previous sections was performed with such goals, and has been focused around new simulation and control technologies useful to improve power quality.

Section 2.1 focuses on discontinuous conduction phenomena identified in two-level voltage source inverters. Discontinuous conduction was shown to happen during the short dead time when both switching transistors of a two-level phase leg are switched off. Such dead times are introduced by the PWM controller at each switch-over to avoid phase leg short circuits. The possible switching states and the resulting current and voltage waveforms were identified and a working solution was shown for compensation of this nonlinear behavior for single phase half bridge inverters. This work has been summarized in Thesis 1, repeated below:

Thesis 1.:

I have shown that discontinuous conduction can happen during effective dead time in single phase half-bridge inverters. I have identified the waveforms of discontinuous conduction during dead time. I have defined a method for estimating the error in the output voltage of a phase leg. I have shown that this estimation can be used for partial analytical compensation of the error in single phase half bridge inverters.

This idea has been researched further to find similar events in the more widely used three phase full bridge topology. This research has shown that the resulting three phase waveforms are much more complex than the single phase ones. The reasons for this are the changes in the

potential of the star point when compared to the DC bus. This had to be thoroughly investigated and the possible voltage and current waveforms had to be found in order to be able to apply the principles of Thesis 1 for three phase systems. The new compensation methods for nonlinearities caused by discontinuous conduction during dead time in three phase systems have been discussed in section 2.2. and summarized as Sub thesis 1.1, repeated below:

***Sub thesis 1.1**:*

I have defined a method for forecasting the values of current ripple for the next switching period of three phase two level inverters. I have shown that by using the forecasted current ripple values it is possible to compensate for the error caused by discontinuous conduction during switching dead time. I have verified the operation of the new dead time compensation method by computer simulation.

It was shown by computer simulations that the analytical methods described in sections 2.1 and 2.2 work well but are computationally intensive. A simpler but effective solution was given for the same problem in section 2.3. This runs a simple model of the inverter which evaluates all possible switching states for a set of duty ratio inputs, including discontinuous ones, and calculates the average inverter output voltages. A compensator based on this idea was shown to result in a better set of duty ratios, resulting in more linear operation. More iterations of the model were shown to increase accuracy. The results of this work were summarized in Sub thesis 1.2, repeated below:

***Sub thesis 1.2**:*

I have defined a model based method for estimating the expectable error of phase leg output voltages in the next switching period of three phase two level VSI. The new method calculates with all switching states within a period. I have shown that this model can be used to achieve more accurate dead time compensation than with using the linear interpolation based method. I have shown that repeated execution of the model increases accuracy.

Section 3 focuses on a new fast simulation method which is capable of simulating discontinuous conduction phenomena such as the ones described in sections 2.1 and 2.2. It was shown that existing models were often too complicated and slow when simulating discontinuous conduction in phase legs containing diodes. Simpler switching function based models better suited for fast off-line or even real-time simulations had different problems also resulting in significant slowdowns and bad results under discontinuous conduction situations. To support research described in section 2, a new model was made which is similar to a switching function based model but also contains a PI controller and works well with discontinuous conduction. The operation if this model was verified using computer simulation. The results of this research were summarized in Thesis 2, repeated below:

Thesis 2.:

I have shown that the output voltage of the switch based phase leg model shows a limit cycle operation during control dead time and when the phase leg is off. I have shown that by including the junction capacitance in the model, discontinuous conduction can already be simulated. I have made a fast phase leg model based on a discrete PI controller. I have shown that the model can approximate well the voltage of the switched point, and that it can be used for the simulation of discontinuous conduction during dead time.

Section 4 focuses on harmonic emissions caused by 60° Flat-Top (DPWM1) modulation in 2-level 3-phase inverters. Flat-Top is a zero sequence PWM modulation method widely used by the industry to increase the efficiency of three phase full bridge inverters. Flat-Top modulation reduces switching losses by not switching the phase leg which conducts the largest current for active loads. The causes of the emissions were investigated for two-level inverters in section 4.1. A simple and effective solution was presented in section 4.2 which works well but loses some of the efficiency gains of the original Flat-Top modulation. The actual waveforms were further researched in section 4.3 to find a possible method which is capable of compensation of this source of harmonic emissions without compromising the advantages of Flat-Top. The actual compensation algorithm has been described in section 4.4 and was tested using measurements on two different inverter setups. The results have been summarized in Thesis 3, repeated below:

Thesis 3.:

I have shown that the output current of 60° FLAT-TOP modulated inverters has an incorrect value for one switching period at every zero sequence step. I have identified the current and voltage waveforms caused by the step in LC filtered three phase inverters. I have shown how to calculate the duty ratios required for minimal distortion in each phase. Based on the resulting formulae, I have defined a method to decrease harmonic emissions caused by FLAT-TOP modulation. I have shown that the efficiency of a converter using the new compensated modulation is not worse than with using the original FLAT-TOP modulation.

5.1. Practical Usability of Research Results

The research of dead time compensation methods described in thesis 1 was performed in cooperation with Siemens Zrt in frame of the eAutoTech projekt (KMR 12-1-2012-0188KMR12), but this project did not get to full realization due to changes within the company.

The further developed versions of the patented simulation method capable of simulating dead time effects described in thesis 2 were and are still being used by the R&D department of Siemens Zrt and its successors in their own HIL simulators.

The FLAT-TOP modulation method described in thesis 3 was applied in a 50kW DC electric car fast charger in cooperation with Procon Drivesystem Ltd.

5.2. Future research topics related to the theses

The distortions caused by discontinuous conduction during dead time as shown in thesis 1, and those caused by FLAT-TOP modulation as shown in thesis 3 are due to transients

appearing at actual phase angles of the fundamental voltage- or current component. These cause low order harmonic currents. The compensation of these has the largest effect on harmonic emissions in situations where the ratio of switching- and fundamental frequencies is relatively low (in the order of 100 or less). Among grid connected converters, these are typically the high power ones, running at switching frequencies at or below 10kHz. During my research, I made simulations and measurements for such converters. In further research, it would be interesting to investigate applications of these methods in drives of modern electric vehicles. As synchronous modulation and fundamental frequencies in the kHz range are becoming increasingly common in high pole number or high RPM motor drives, the detailed compensation methods can have a significant effect on the harmonic content of motor currents and on the efficiency of such drives.

The actual work described in this dissertation was focused on traditional two-level topologies. The applicability of the methods described in the theses for multilevel topologies could be further researched. As an example, the 3-level NPC topology inverters can in most cases directly replace 2-level inverters, and can have similar – albeit more complicated – problems with dead time, discontinuous conduction, and discontinuous PWM modulations similar to Flat-Top.

The topic of discontinuous conduction and appropriate control methods also require further research in special PFC topologies including various types of bridgeless rectifiers. Such topologies are being increasingly used in single phase power supplies and on-board battery chargers because they can be built using a smaller number or lower voltage semiconductors and can have better efficiency and lower cost than traditional PFC topologies.

Probably the most successful three-level PFC topology used in three phase systems is the Vienna rectifier. Such converters are also becoming widespread in e-car chargers for the same reasons described above, and this topology also has additional benefits from being a three-level topology. The problem of discontinuous conduction at zero-crossings and reactive power balance are complicated problems with such converters affecting EMC and requiring further research.

List of own publications

Journal papers:

[J1] **Andras Futo**, Istvan Varjasi, „Compensation of Discontinuous Conduction in Three Phase Voltage Source PWM Inverters," ***RENEWABLE ENERGY & POWER QUALITY JOURNAL*** vol. 1, no. 12, pp. 425-430, Apr. 2014, DOI: 10.24084/repqj12.356

[J2] **Andras Futo,** Tamas Kokenyesi, Istvan Varjasi, Zoltan Suto, Istvan Vajk, Attila Balogh, Gergely Gyorgy Balazs, „Real-Time HIL Simulation of the Discontinuous Conduction Mode in Voltage Source PWM Power Converters," ***JOURNAL OF POWER ELECTRONICS*** (IF: 0.901, Q2), vol. 17, no. 6, pp. 1535-1544, Nov. 2017

[J3] **Andras Futo**, Istvan Varjasi, Istvan Vajk, Rafael Kalman Jardan, "Analytical Compensation of Harmonics caused by 60° Flat-Top Modulation," ***IET POWER ELECTRONICS*** (IF: 2.839, Q1), vol. 12, no. 7, pp. 1763-1773, Mon. 2019, DOI: 10.1049/iet-pel.2018.5855 , ISSN: Print: 1755-4535, Online: 1755-4543

Patents:

[P1] **Andras Futo**, Istvan Varjasi, Tibor Debreceni, Gergely Gyorgy Balazs METHOD AND SYSTEM FOR DEAD TIME COMPENSATION IN A PWM CONTROLLED INVERTER, EP3104516 , Submission Year: 2015, Submission Number: 15462001.7 , Country of patent: Hungary

[P2] Tamas Kokenyesi, Istvan Varjasi, Tibor Debreceni, Gergely Gyorgy Balazs, **Andras Futo**, METHOD AND SYSTEM FOR SIMULATING INVERTER PHASE LEGS DURING DISCONTINUOUS CONDUCTION MODE, EP3104514 , Submission Year: 2015 , Submission Number: 15462001.7 , Country of patent: Hungary

Conference papers:

[C1] **Andras Futo**, „Discontinuous Conduction in Grid Connected Voltage Source Inverters," in *Proc. Automation and Applied Computer Science Workshop AACS '13*, 2013, Budapest, Hungary, pp. 130-139.

[C2] **Andras Futo**, Istvan Varjasi, „Compensation of discontinuous conduction in single phase grid connected PWM inverters," in *Proc. 13th Int. Conf. on Environment and Electrical Engineering (EEEIC '13)*, 2013, Wrocław, Poland, pp. 126-131.

[C3] **Andras Futo**, Istvan Varjasi, Zoltan Suto, „Current Ripple Calculation for Dead Time Compensation in Three Phase PWM Inverters," in *Proc. IEEE International Energy Conference (EnergyCon '14)*, 2014, Dubrovnik, Croatia, pp. 195-201.

[C4] **Andras Futo**, Istvan Varjasi, „Simple Model Based Dead Time Compensation Using Fast Current Measurement," in *Proc. AASRI Conference on Circuit and Signal Processing (CSP '14)*, 2014, London, UK, pp. 146-151.

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